Prime Computer Logic Diagrams

SYSTEM OPTION CONTROLLER

W.W./E.V.

LOGIC DIAG. LDS1627

Prime Computer, Incorporated, 145 Pennsylvania Avenue, Framingham, Massachusetts 01701

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1.0 GENERAL DESCRIPTION

The SOC is intended to perform the functions of the Option A plus several new ones. The board will contain:

1. Asynchronous Serial Line Control on one of four multiplexed lines with independent transmit/receive. This will interface the system console device (ASR, CRT,...) and the other serial EIA peripheral devices we now offer.

2. Synchronous Serial Line Control on one of four multiplexed lines.

3. Two sixteen-bit (or optionally eight-bit byte packed) half duplex Buffered Parallel Input/Output Channels. These will interface our paper tape (reader and punch) peripherals and some of the other parallel TTL peripheral devices we now offer.

4. The ability to have any or all of the above options use DMA/C with programmable channel address.

5. A line frequency clock.

6. A programmable interval clock with a resolution of 3.2 usec or 102.4 usec (under program control).

7. A Watch-Dog Timer.

Each of these components is described in a separate section.

2.0 APPLICABLE DOCUMENTS

PRIME I/O Bus Specification PE-T-42
PRIME 200 CPU Specification

3.0 OPERATING CHARACTERISTICS

The SOC consists of four controllers which share the standard I/O interface. The various controllers can be operated independently of each other. They are all operable in PIO mode for the transfer of control and status information and for the transfer of data. PIO mode includes interrupt control (vectored or standard) with programmable interrupt vectors.

The implementation of interrupt control is such that any interrupt that occurs will hold off its own and all other interrupts from SOC until the interrupt has been acknowledged (CAI).

I-01	USED ON	SCALE	SIZE	DWG. NO.	REV.
	NEXT ASSY	SHEET 2 OF 48		SPC 1831	

PDF-005

MATERIAL	DWN	PRIME COMPUTER INC. NATICK, MASS.			
	CHK				
UNLESS OTHERWISE SPECIFIED -REMOVE ALL BURRS AND SHARP EDGES -DIMENSIONS ARE IN INCHES -TOLERANCES xx ±.02 xxx ±.005 ANGLES ±1/2°	ENG.	SYSTEM OPTION CONTROLLER (SOC) FUNCTIONAL SPECIFICATION			
	APPRD				
	USED ON	SCALE	SIZE	DWG. NO.	REV
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The three peripheral controllers (excluding the clock) may transfer data via DMA/C.

The DMA/C control section samples each controller to determine whether there is a pending request. Upon detecting a request, the control section activates the standard DMA/C I/O control section on behalf of the requesting controller. At the end of the transfer, the control continues its scan. The sample rate is 5 MHZ. This means that the SOC can never use the I/O bus for two consecutive DMA/C transfers.

3.1 Asynchronous Serial Line Controller (ASLC)

The ASLC can be used to interface to asynchronous serial communications line operating to 9.6 KB (Kilo-Baud). The detailed format of the information and the particular operating speed are under program control and may be independently specified for receive mode and transmit mode.

The ASLC consists of two control sections (one for receive and one for transmit) and a line interface. The line interface can be connected to up to four asynchronous serial communications lines or up to four local peripheral devices if the devices follow the serial communications discipline implemented. Since there is only one control section for each direction of information flow, only one communications line or one local peripheral may be operating at a given time in a given direction. However, since the line selected is under program control, several lines or devices may be connected and used in a serial fashion. Thus, one could print a line on a serial printer and then punch a card on a serial card punch or simultaneously read a card and print a line.

The software can select the following parameters for the data format independently for receive data and transmit data:

1. character length - 5, 6, 7 or 8 bits

2. number of stop bits - 1 or 2 (1-1/2 for character length of 5)

3. parity - even or odd or none

The bit rate (baud) which is programmable, is provided by a clock operating at sixteen times the desired rate.

In addition to the data transfer lines, there are additional signals which can be controlled and sampled to facilitate interfacing the ASLC to a communications line or a peripheral device. The signals might be used for clear to send or data terminal ready.

There are four signals (one from each line) which can be sampled and there are four signals (one for each line) which can be controlled. Two of these are controlled by the receive section and two by the transmit section.

The line discipline implemented is EIA compatible RS 232-C for all data and control signals. In addition each of the transmit data lines is provided with 20 ma current loop capability and receive line 1 is provided with the same current loop capability.

The lines are arranged so that receive line 1 and transmit line 1 can be used by a TTY as the system console.

Both the receive and transmit control sections may be operated in programmed I/O mode and interrupt mode. In interrupt mode there is one programmable interrupt vector location for each control section.

When DMA/C is used (see 3.4), each of the control sections is provided with one channel.

3.2 Synchronous Serial Line Controller (SSLC)

The SSLC can be used to interface to a synchronous serial communications line operating to 19.2 KB* (Kilo-Baud). The detailed format of the information and the particular operating speed are under program control and may be independently specified for receive mode and transmit mode.

The control section of the SSLC is identical to that described for the ASLC (see section 3.1) except that stop bits are not used and the method of clocking differs. The SSLC is usually operated with an externally provided modem clock at the desired baud. The SSLC is also provided with an internal clock for test purposes.

The receive section of the SSLC is provided with the capability to enter a "Search for Sync" mode of operation. In this mode the SSLC will search for a match between an incoming bit stream and a programmed sync character. The SSLC will search for two consecutive sync characters and then strip all succeeding lead sync characters. Once the message (one non-sync character) is begun, the SSLC will leave search for sync mode and faithfully provide all characters.

There are a total of two control sections, either of which may be operated in an asynchronous mode or a synchronous mode. Thus, the addition of the synchronous capability does not increase either the total number of lines that can be controlled (four receive and four transmit) nor the number of lines that can simultaneously be operated (one receive and one transmit).

*See Appendix A

3.3 Buffered Parallel Input/Output Channel (BPIOC)

The SOC is provided with one or two BPIOC's. Each BPIOC can operate as an eight-bit, eight-bit byte packed, or sixteen-bit half-duplex channel. The byte-packing is program selectable.

Each BPIOC can use up to 16 data lines and 6 control lines. The control lines can be levels or pulses of either polarity.

The SOC is normally provided with the BPIOC configured to perform a particular function: a) interface to a Paper Tape Reader (PTR); b) interface to a Paper Tape Punch (PTP); c) general purpose interface with a hand shake interface (see 4.3 for details).

3.3.1 PTR

When the BPIOC is used to provide an interface to a Remex Paper Tape Reader, data are input a byte at a time. In normal mode (full-word) the left byte is set to a 0 and the data inserted in the right byte. In byte-pack mode, the first datum appears in the left byte and the second is in the right byte. The PTR interface uses positive true (+T) data and negative true control signals (-T).

3.3.2 PTP

The BPIOC, when used to provide an interface to a Remex Paper Tape Punch, outputs data a byte at a time. In normal mode (full-word), the right byte is the one transferred. In byte-pack mode, the first byte is the left byte followed by the right byte. Data is +T and the control signals are +T.

3.3.3 BPIOC

When the BPIOC is used as a general purpose interface, the transfer of data is determined by the user. Data may flow a byte at a time or a 16-bit word at a time. The data is +T and the control signals are -T.

3.3.3.1 Byte Transfer

The BPIOC will input a single byte and right justify it with 0's on the left. When performing byte-packing, the first byte is left justified and the second byte inserted on the right prior to transfer to the CPU.

In output mode, a single byte will be transferred from the right (the left byte is ignored). When in byte-pack mode, the left byte is transferred first followed by the right byte.

Each BPIOC may be independently operated in the programmed I/O mode, interrupt mode, or DMA/C mode.

3.4 DMA/C - Programmable Channel Address

This feature provides four programmable DMA/C channel address registers (CAR) and the control logic for the ASLC (SSLC) and the BPIOC('s) to operate via DMA/C. Each CAR can be independently programmed; one is for the receive section of the ASLC/SSLC; one for the transmit section; and one for each BPIOC.

The DMA/C may be enabled under program control for each option. Data transfers will continue on each of the enabled sections (up to four simultaneously) until the CPU informs the channel that an end of range (EOR) has occurred. The particular option that gets EOR will cease DMA/C data transfers and will interrupt the CPU. Meanwhile, the remaining options will continue their data transfers.

3.5 Line-Frequency Clock

The line-frequency clock will operate at 60 or 50 cps. When enabled, each cycle of the line-voltage will result in a memory cell being incremented. The particular cell used is programmable. When the value of the cell is incremented from -1 to 0, an interrupt will be generated. There is also a provision for an externally provided clock to be used for the memory increment. The LFC uses super-hi priority interrupts for the memory increment.

3.6 Programmable Interval Clock (PIC)

The PIC can be programmed to time an interval of up to 200 msec with a resolution of 3.2 usec or 6.7 sec with a resolution of 102.4 usec. The current value of the PIC is available to the program. When the internal has ended, the PIC can be programmed to use the line-frequency memory increment or to cause an interrupt or both. The interrupt vector is identical to that used by the line-frequency clock and is differentiated from it by a sense instruction (see section 4.4).

3.7 Watch-Dog Timer (WDT)

The WDT is provided with the ability to perform a system reset function (similar to depressing the control panel Master Clear switch) followed by an auto-restart/auto-load. The WDT can also provide an isolated contact closure which can be used to signal the external world.

The WDT will perform the above functions in one of two cases: 1) A period of 50 msec during which the program has failed to acknowledge the WDT (time-out); 2) The occurrence of a loss of power.

The system reset at the end of the time-out is under program control In either case, the system reset can be externally initiated by connection of a contact closure to the WDT.

The WDT is provided with four external lines. Two of these signal a time-out and the other two are used to initiate a system reset/auto-load.

4.0 PROGRAMMING

4.1 ASLC

The ASLC has two distinct operating modes. The first mode is the "Compatible" mode of operation and is entered with a system reset, OCP initialize ('17), OCP set to Input Mode ('00), and OCP set to Output Mode ('01).

While in this mode of operation, the receive and transmit portions can only be operated one at a time. The ASLC is placed in "echo-plex" mode. The half which is not enabled does not function. Thus if in "Compatible-Input" mode, an OTA data ('00) will never succeed. In addition, only the enabled half can generate interrupts or DMA/C data transfers. The interrupt vector used will be the receive vector in "Compatible-Input" mode and the transmit vector in "Compatible-Output" mode.

The ASLC has one interrupt mask in the "Compatible" mode which may be set [OCP set mask ('15)] or reset [OCP reset mask ('16)] under program control.

The ASLC may also be used with both receive and transmit enabled [OCP enable Input and Output ('12)]. This command also takes the ASLC out of the diagnostic mode.

In this mode, receive and transmit are independent. The interrupt masks and DMA/C enable are separate. The receive mask may be enabled or disabled and DMA/C may be enabled or disabled. Similarly for the transmitter.

In addition to these controls, there are two control registers (CR) for receive and two for transmit. They are organized as follows:

Control Register 1

Bits 1 + 2: Control Bits 1 and 2. For receive, these are provided on lines 1 and 2. For transmit, these are provided on lines 3 and 4.

Bits 3 + 4: Port Select - 1 of 4

Bits 5-16: Clock Speed. The value is calculated using:

$$N = 4096 \times \frac{16}{5} \times CS \times 10^{-6}$$

where N is the 12 bit speed select. For the ASLC, CS is 16 X Baud. For the SSLC, CS is Baud (see 5.2.1.1 for common rates).

Control Register 2

Bit 1: Must be zero (MBZ)

Bit 2: Number of stop bits - a 0 sets 1 stop bit; a 1 sets 2 stop bits. (1-1/2 for 5-bit characters)

Bits 3 + 4: Character length as follows:

00	5 bits
10	6 bits
01	7 bits
11	8 bits

Bit 5: Parity inhibit - the parity bit when enabled is added to the number selected by bits 3 and 4.

Bit 6: Select even parity (a 0 selects odd parity)

Bits 7-16: MBZ

The control registers are available to the program for reading (see 4.1.4). However, following an Initialize (OCP '17, OCP '00, OCP '01, and Master Clear), the value read is not correct (This is due to the characteristics of the Registers used to contain the information). The value used to determine line parameters are, however, correct as specified in section 4.1.4.1. A sense instruction has been added which provides information as to the validity of the registers read. The registers read become valid once changed by the program.

The ASLC is initialized into "Echo-plex" mode. It may be operated in "Full-Duplex" mode under software control.

The ASLC can be operated in Diagnostic mode where the transmitter is looped back to the receiver.

4.1.1 ASLC Command Description

The standard device address of the ASLC is '04.

4.1.2 OCP Instructions

4.1.2.1 OCP '0004

This will set the ASLC into "Compatible-Input" mode. Thus the ASLC will respond ready (PIO, Interrupt or DMA/C) only when a character is received.

This instruction also resets both the Input and Output port select so that Port 1 is selected and resets the clock speed so that 110 baud is selected. Also, two stop bits, 8 bit character length and parity disabled are selected.

4.1.2.2 OCP '0104

This will set the ASLC into "Compatible-Output" mode. The ASLC will only respond ready when a character has been transmitted. As the ASLC transmitter is double buffered, the time between the first two characters of a message will correspond to several clock periods and not a full character time. This instruction performs the same resets that OCP '0004 does.

4.1.2.3 OCP '0204

Set Receive Interrupt Mask.

4.1.2.4 OCP '0304

Enable Receive DMA/C operation. This flag is automatically reset when Receive End of Range is detected.

4.1.2.5 OCP '0404

Reset Receive Interrupt Mask and Reset Receive DMA/C.

4.1.2.6 OCP '0504

Set Transmit Interrupt Mask.

4.1.2.7 OCP '0604

Enable Transmit DMA/C operation. This flag is automatically reset when Transmit End-of-Range is detected.

4.1.2.8 OCP '0704

Reset Transmit Interrupt Mask and Reset Transmit DMA/C.

4.1.2.9 OCP '1004

Enable Input and Output "Full-Duplex". This takes the ASLC out of "Echo-plex" mode and puts it into "Full-Duplex" mode (see 4.1.2.10).

4.1.2.10 OCP '1104

This instruction is used in Diagnostic mode to provide an oscilloscope synchronizing pulse.

4.1.2.11 OCP '1204

Enable Input and Output "Echo-plex". This takes the ASLC out of "Compatible" mode and allows independent receive and transmit operations. This also takes the ASLC out of Diagnostic mode.

4.1.2.12 OCP '1304

Set Diagnostic Mode. This enables the output of the transmit section to be looped back to the receive section.

4.1.2.13 OCP '1504

Set Interrupt Mask. This is a "Compatible" mode instruction and causes both the receive and transmit interrupt masks to be set.

4.1.2.14 OCP '1604

Reset Interrupt Mask. This instruction resets both the receive and transmit interrupt masks.

4.1.2.15 OCP '1704

Initialize. This sets "Compatible-Input" mode (see 4.1.2.1) and resets all interrupt masks and all DMA/C enables.

4.1.3 SKS Instructions

4.1.3.1 SKS '0004

Skip if Ready

This instruction tests ready if:

- Compatible Input Mode and Character Received
- Compatible Output Mode and Transmitter Ready for reset character
- Input and Output Mode and either of the above

4.1.3.2 SKS '0104

Skip if Not Busy

This instruction tests ready if:

- Compatible Input Mode and no character being received
- Compatible Output Mode and no character being transmitted
- Input and Output Mode and neither of the above

4.1.3.3 SKS '0204

Skip if Receiver not Interrupting

4.1.3.4 SKS '0304

Skip if Control Registers Read are Valid

This tests false following Master Clear OCP Input ('00), OCP Output ('01) and OCP Initialize ('17). This is set by an OTA Receive Control Register 1 ('04).

4.1.3.5 SKS '0404

Skip if neither Receiver nor Transmitter Interrupting

4.1.3.6 SKS '0504

Skip if Transmitter not Interrupting

4.1.3.7 SKS '0604

Skip if Transmitter Ready for next character and not Compatible Input Mode.

4.1.3.8 SKS '0704

Skip if Receiver Ready (character received) and not Compatible Output Mode.

4.1.3.9 SKS '1104

Skip if Input Bit 1 is Marking (+12v). An open line is treated as a space.

4.1.3.10 SKS '1204

Skip if Input Bit 2 is Marking

4.1.3.11 SKS '1304

Skip if Input Bit 3 is Marking

4.1.3.12 SKS '1404

Skip if Input Bit 4 is Marking

4.1.3.13 SKS '1504

Skip if Parity Error

This happens if the received character has incorrect parity.

4.1.3.14 SKS '1604

Skip if Overrun Error on Receive

This happens if a second character is completed prior to the first being taken by an INA.

4.1.3.15 SKS '1704

Skip if Framing Error

This happens if there is no stop bit where one is expected.

The three error conditions ('15, '16, '17) are accumulated on a message basis. Thus, they are reset by a Load Receive Control Register 1 instruction.

4.1.4 INA Instructions

4.1.4.1 INA '0004

Input received character if the receiver is ready and the ASLC is not in "Compatible-Output" mode. The character is

in the right byte with the left byte set to 0. The character is "OR-ed" into the CPU A Register. The INA resets receive ready. The parity bit (if enabled) appears as the leftmost bit. Since only 8 bits are sent to the CPU, the 9th bit (8 bits and parity) is lost.

4.1.4.2 INA '0404

Input Receive Control Register 1 (see SKS '03 to determine if valid)

4.1.4.3 INA '0504

Input Receive Control Register 2

4.1.4.4 INA '0604

Input Transmit Control Register 1

4.1.4.5 INA '0704

Input Transmit Control Register 2

4.1.4.6 INA '1004

Same as INA '0004 except that CPU A register is set to 0 prior to Input.

4.1.4.7 INA '1104

Input ID. This instruction is always ready. The ID of the ASLC is '104.

4.1.4.8 INA '1404

Input Receive DMA/C channel address

4.1.4.9 INA '1504

Input Transmit DMA/C channel address

4.1.4.10 INA '1604

Input Receive Interrupt Vector

4.1.4.11 INA '1704

Input Transmit Interrupt Vector

4.1.5 OTA Instructions

4.1.5.1 OTA '0004

Output character to be transmitted if the transmitter is ready and the ASLC is not in "Compatible-Input" mode. The character is taken from the right byte and is right justified. The OTA resets transmit ready.

4.1.5.2 OTA '0404

Output Receive Control Register 1

4.1.5.3 OTA '0504

Output Receive Control Register 2

4.1.5.4 OTA '0604

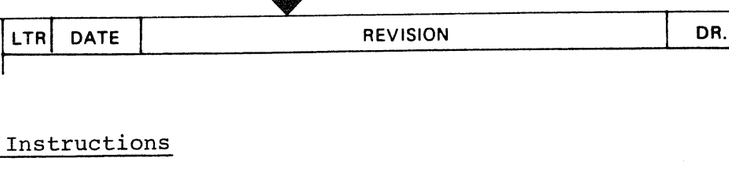
Output Transmit Control Register 1

4.1.5.5 OTA '0704

Output Transmit Control Register 2

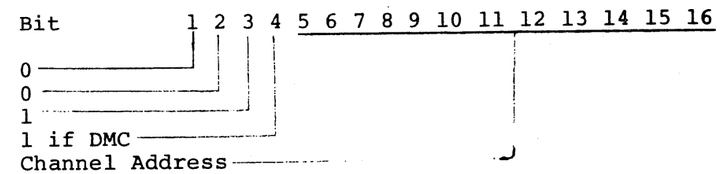
4.1.5.6 OTA '1404

Output Receive DMA/C channel address. The format is as follows:



4.1.5.7 OTA '1504

Output Transmit DMA/C channel address. The format is as follows:



4.1.5.8 OTA '1604

Output Receive Interrupt Vector. Bits 1-4 must be 0.

4.1.5.9 OTA '1704

Output Transmit Interrupt Vector. Bits 1-4 must be 0.

4.1.6 Interrupts

Interrupts are generated in two situations. When either the receive or transmit section is in PIO mode (not DMA/C), the occurrence of the ready condition in conjunction with the interrupt mask results in an interrupt. In DMA/C mode, the occurrence of the ready condition results in a DMA/C request being generated. When DMA/C End of Range is detected, PIO mode is entered and the ready condition is forced on. This results in an interrupt being generated.

4.2 SSLC

The SSLC includes all the functions of the ASLC. However, one new command is implemented which enables "Search for Sync", and new bits are added to Control Registers 2.

Search for Sync mode is entered by resetting the receiver (OCP '404), setting the interrupt mask and DMA/C if desired, setting the Sync character (see below), and issuing the enter Search for Sync mode instruction (OCP '14). The receiver begins comparing the input bit stream with the desired Sync character. When a match is detected, the receiver examines the next character to see if it is also a Sync character. If it is not, the receiver once again enters its bit stream comparison mode. When the second character is a Sync, the receiver continues ignoring all successive Sync's. When the first non-Sync character is received, the receiver leaves the Search for Synch mode and sets its ready condition so that the CPU can take the received character.

The SSLC can be operated in Diagnostic mode as the ASLC can. Also, the Diagnostic mode causes the SSLC to use the internal clocks instead of the external modem clocks.

Control Register 2

Bit 1: Sets Synchronous Mode

Bit 2: Number of stop bits (see ASLC). This must be 0 for Synchronous mode.

Bit 3-8: Same as ASLC

Bits 9-16: Receive - Sync character
Transmit - Fill character

The SSLC transmitter will place the Fill character on the line if the CPU does not provide a character when needed.

4.2.1 SSLC Command Description

The standard device address of the SSLC is '04. Only those commands which are different from those of the ASLC are listed.

4.2.2 OCP Instructions

4.2.2.1 OCP '1404

Set Search for Sync mode

4.2.3 SKS Instructions

4.2.3.1 SKS '1004

Skip if not in Search for Sync mode

4.3 BPIOC

The BPIOC section controls the 16 data lines and 6 control signals. The control signals are assigned so that three are Input and three are Output. The Input lines are as follows:

a. A device status line which may be sampled (SKS '01)

b. A device ready line

c. A device data strobe line

The Output lines are as follows:

a. A device enable line which comes from the control register (OTA '07)

b. A data strobe line for forward mode

c. A data strobe line for reverse mode

The BPIOC can be set (via hardware) so that it is initialized in either the Input or the Output mode. In addition, there are 13 parameters that are hardware specified.

They are:

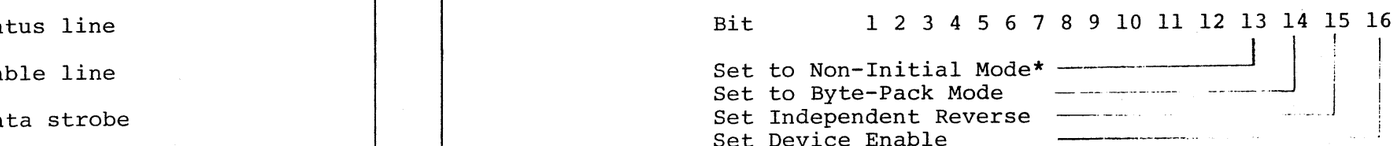
1. The polarity of the device readyline
2. The polarity of the device strobe line
3. The polarity of the device status line
4. The polarity of the device enable line
5. The polarity of the forward data strobe
6. The polarity of the reverse data strobe
7. Whether the data strobes are pulses or levels
8. Whether the data strobes are independent or not. One mode sets them so that both may occur simultaneously. Where the first is enabled by the forward/reverse flop and the second is enabled by the independent reverse flop. The other mode enables them with opposite polarities of the forward/reverse flop.
9. The edge of the device ready line to use
10. The edge of the device strobe line to use
11. The pulse width of the data strobes
12. The time between device strobe and the acceptance of data in Input mode and the time between data stable and data strobe in Output mode.
13. The time between the generation of device ready and the generation of data strobe in Input mode. The time between device strobe and data strobe in Output mode.

All of the Input control lines are pulled up via a 1K resistor to +5 and are received by Schmitt triggers. All Output control lines are driven by 7404's.

All Input data lines are pulled up via 1K resistors to +5 and all Output data lines are driven by 74 H01. See Appendix B for recommended circuit connection.

When the BPIOC is used in the Byte Pack mode, the most significant byte is dealt with first. On output, the left byte followed by the right byte are output. On input, the first byte received is placed in the right byte of the holding register. When the second byte is received, the first byte is transferred to the left byte of the data register and the new byte is placed in the right byte.

The Control Register has bits assigned as follows:



The BPIOC is available in three standard configurations: as a Paper Tape Reader (PTR); as a Paper Tape Punch (PTP); and as a BPIOC. For each of these configurations, the hardware parameters are pre-set. The following sections describe these configurations.

4.3.0.1 Paper Tape Reader

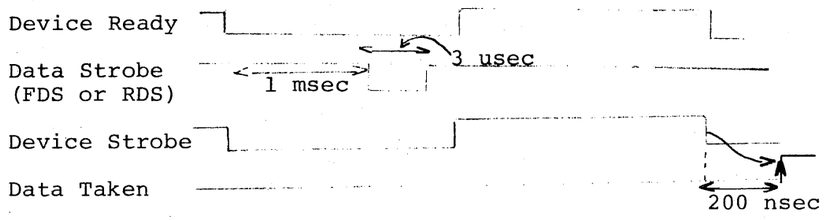
1. The Device Ready Line is -T.
2. The Device Strobe Line is connected to the Device Ready Line.
3. The Device Status Line is -T and indicates power on, unit available and tape ready.
4. The Device Enable Line is not used.
5. The Forward Data Strobe is -T.
6. The Reverse Data Strobe is -T.
7. The Data Strobes are pulses.
8. The Data Strobes are dependent (controlled by OCP FORWARD/REVERSE - one at a time).
9. The lead edge of Device Ready initiates the next Data Strobe (FWD or RVS).
10. The trail edge of Device Strobe is used to indicate that data is available.

*Set Input if Output is initial
Set Ouput if Input is initial

11. The Data Strobes are 3 usec pulses.

12. Data is accepted 200 nsec. following the trail edge of Device Strobe.

13. Data Strobe (FDS or RDS) occurs 1 msec following the lead edge of Device Ready.



4.3.0.2 Paper Tape Punch

1. The Device Ready Line is +T.

2. The Device Strobe is +T.

3. The Device Status is -T.

4. The Device Enable is not used.

5. The Forward Data Strobe is not used.

6. The Reverse Data Strobe is not used.

7. The Data Strobe is a pulse.

8.

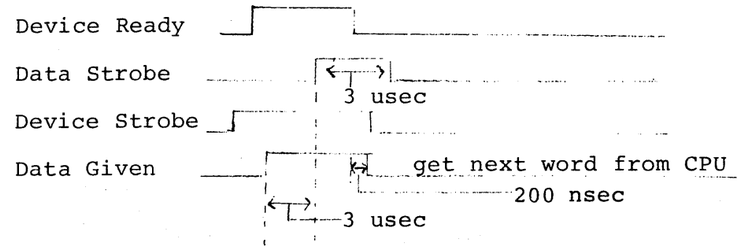
9. The lead edge of the Device Ready Line is used.

10. The trail edge of the Device Strobe is used.

11. The Data Strobe is a 3 usec pulse.

12. There are 3 usec between Data Stable and Data Strobe.

13. There are 3 usec between Device Ready and Data Strobe.



4.3.0.3 BPIOC

1. The Device Ready Line is -T.

2. The Device Strobe is -T.

3. The Device Status is -T.

4. The Device Enable is -T.

5. The Forward Data Strobe is -T.

6. The Reverse Data Strobe is -T.

7. The Data Strobes are levels (hand shake).

8. The Data Strobes are independent. Either one or both may be generated as follows:

Forward/Reverse Flop (OCP)	Independent Reverse (OTA)	Result
FWD (OCP 02)	OFF (0)	FDS
RVS (OCP 03)	OFF	none
FWD	ON (1)	FDS and RDS
RVS	ON	RDS

9. The lead edge of Device Ready allows operation.

10. Input: The lead edge of strobe says here's data.
The trail edge says end of transfer.

Output: The lead edge of strobe says give me data.
The trail edge says I've got it.

11.

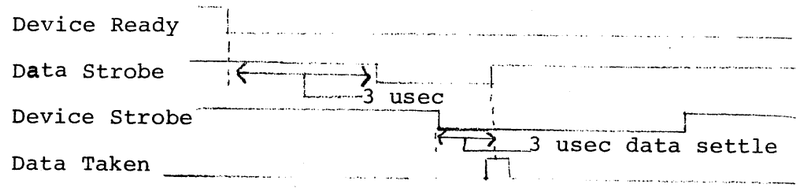
12. Input: Data is taken 3 usec following the lead edge of Device Strobe.

Output: Data Strobe is generated 3 usec after data is put on the data lines.

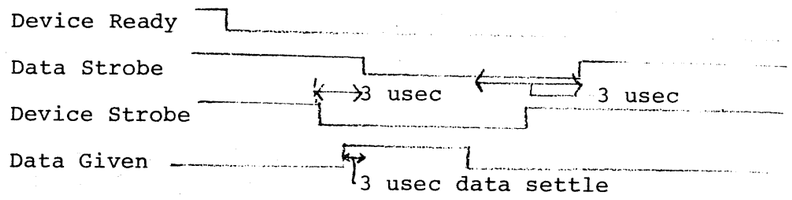
13. 3 usec for both.

The BPIOC is initialized in Input mode.

Input



Output



4.3.1 BPIOC Command Description

The standard device addresses (XX) are as follows:

PTR	'01
PTP	'02
BPIOC #1	'30
BPIOC #2	'31

4.3.2 OCP Instructions

4.3.2.1 OCP '00XX

Start. This enables the BPIOC to transfer data, resets the data register, and resets the right-byte-next flag.

4.3.2.2 OCP '01XX

Stop. This prevents further data transfer. The BPIOC must be stopped prior to a direction switch and prior to a control register change.

4.3.2.3 OCP '02XX

Forward. This sets the forward/reverse flop.

4.3.2.4 OCP '03XX

Reverse. This resets the forward/reverse flop.

4.3.2.5 OCP '14XX

DMA/C. This enables DMA/C mode.

4.3.2.6 OCP '15XX

Set Interrupt Mask.

4.3.2.7 OCP '16XX

Reset Interrupt Mask.

4.3.2.8 OCP '17XX

Initialize. This sets Stop and Forward. This resets the data register, right-byte-next, Interrupt Mask, DMA/C enable, and the control register (non Byte-Pack, reset Independent Reverse and reset Device Enable). The BPIOC is initialized in Input mode.

4.3.3 SKS Instructions

4.3.3.1 SKS '00XX

Skip if Ready

This tests ready if:

- Input mode and a word has been received (2 bytes if byte pack)
- Output mode and the device has been given a word (2 bytes if byte pack)
- DMA/C End-of-Range has been received

4.3.3.2 SKS '01XX

Skip if device status line true.

4.3.3.3 SKS '02XX

Skip if right-byte-next flag is set.

4.3.3.4 SKS '04XX

Skip if BPIOC not interrupting. The BPIOC will interrupt, if it is ready, in PIO (non-DMA/C) mode and has its mask set.

4.3.4 INA Instructions

4.3.4.1 INA '00XX

Input data register if ready and Input mode and "OR" with A. The INA resets ready.

4.3.4.2 INA '10XX

Same as INA '00 except that A is cleared prior to the operation.

4.3.4.3 INA '11XX

Input ID. The ID of BPIOC(a) is ('101). The ID of BPIOC(b) is ('102).

4.3.4.4 INA '14XX

Input DMA/C channel address.

4.3.4.5 INA '16XX

Input Interrupt Vector

4.3.5 OTA Instructions

4.3.5.1 OTA '00XX

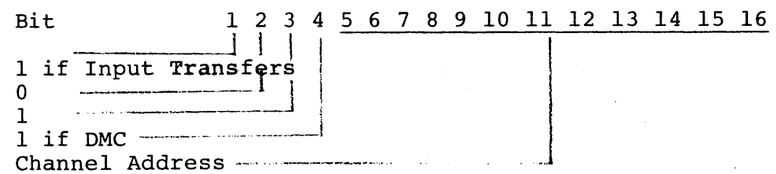
Output A to data register if ready and Output mode. The OTA resets ready.

4.3.5.2 OTA '10XX

Output Control Register

4.3.5.3 OTA '14XX

Output DMA/C channel address. The format is as follows:



4.3.5.4 OTA '16XX

Output Interrupt Vector. Bits 1-4 must be 0.

4.4 Line-Frequency Clock/PIC/WDT

4.4.1 Line-Frequency Clock

The Line-Frequency clock can be controlled using the 60 or 50 Hz AC power line or an externally provided clock. Each period of the clock results in a programmable memory cell being incremented. When the value of memory cell changes from -1 to 0, an interrupt is generated if enabled.

There is a Control Register which is described in section 4.4.4.

4.4.2 PIC

The PIC is a 16-bit counter which can be pre-set and read back. Its clock can be either 3.2 usec or 102.4 usec. The end of an interval can cause a memory increment or an interrupt or both.

4.4.3 WDT

The WDT should always be stopped when power is applied as system reset does not reset the internal registers.

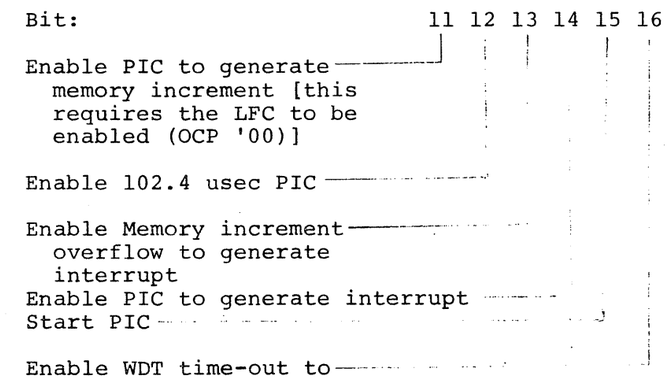
When the WDT time-out occurs, a powerfail interrupt is generated prior to the system reset. Between powerfail and system reset (1 msec) a flag is available on the WDT to indicate that it is responsible. This flag is valid after auto restart/auto load until the WDT is stopped (OCP '07).

When the system reset is initiated by a contact closure, the WDT will continue to generate system resets until the closure is removed. This may result in multiple powerfail interrupts and multiple auto restart/auto loads.

The output contact closure provided in the event of a time-out can sustain 50 milliamperes at 25 volts, non-inductive. The contact is "closed" during normal operation. An error is signaled by a high impedance "open".

The system reset closure must provide 15 milliamperes at 5 volts for 100 usec.

4.4.4 Control Register



4.4.5 LFC, PIC and WDT Command Description

The standard device address of these three options is '20. As a result, the INA and OTA instructions never skip. The controller is always ready for INA and OTA.

4.4.6 OCP Instructions

4.4.6.1 OCP '0020

Start LFC and enable memory increment. This enables the memory increment function and acknowledges the previous memory increment and overflow interrupt.

4.4.6.2 OCP '0120

Acknowledge PIC interrupt

4.4.6.3 OCP '0220

Stop LFC and disable memory increment. This disables the memory increment function and acknowledges the previous memory increment overflow interrupt.

4.4.6.4 OCP '0420

Select Line Frequency for memory increment.

4.4.6.5 OCP '0520

Select external clock for memory increment. When both external clock and PIC are selected for memory increment, a diagnostic mode is enabled whereby any OTA to this controller results in a memory increment.

4.4.6.6 OCP '0620

Trigger WDT. This starts the 50 millisecond time-out if the WDT was stopped and restarts a new 50 millisecond time-out if the WDT was running.

4.4.6.7 OCP '0720

Stop WDT.

4.4.6.8 OCP '1520

Set Interrupt Mask

4.4.6.9 OCP '1620

Reset Interrupt Mask

4.4.6.10 OCP '1720

Initialize. This acts like a system reset. The following things happen:

- LFC stopped
- Line-Frequency selected for memory increment
- Memory increment overflow selected to generate interrupts
- Interrupt Mask reset
- PIC disabled (stopped)
- 3.2 usec clock selected
- PIC disabled from causing interrupts
- WDT disabled from allowing time-outs to generate system resets

4.4.7 SKS Instructions

4.4.7.1 SKS '0020

Skip if not interrupting

4.4.7.2 SKS '0220

Skip if interrupt is not due to memory increment overflow (-1 to 0)

4.4.7.3 SKS '0520

Skip if WDT timed out

4.4.7.4 SKS '0720

Skip if WDT caused powerfail interrupt

4.4.8 INA Instructions

4.4.8.1 INA '0220

Input PIC clock register

4.4.8.2 INA '1120

Input ID. The ID of this option is '120

4.4.8.3 INA '1220

Input memory increment cell address

4.4.8.4 INA '1320

Input Interrupt Vector

4.4.9 OTA Instructions

4.4.9.1 OTA '0220

Set Interval Register. The number entered is the 2's complement of the number of counts prior to overflow. The PIC automatically sets itself up again so that consecutive intervals do not require the software to reset the interval register.

4.4.9.2 OTA '0720

Load control register

4.4.9.3 OTA '1220

Load address of memory cell to be incremented. Bits 1-4 must be 0.

4.4.9.4 OTA '1320

Load Interrupt Vector. Bits 1-4 must be 0.

5.0 SUMMARY

5.1 Command Summary

5.1.1 ASLC/SSLC

Device Address = '04
ID = '104

Op Code / Fctn Code	OCP	SKS	INA	OTA
00	Set to Input mode	Skip if Ready	Input Character and "OR" to A	Output Character
01	Set to Output mode	Skip if Not Busy		
02	Set receive interrupt mask	Skip if receive not interrupting		
03	Set receive DMA/C	Skip if control registers valid		
04	Reset receive interrupt mask and DMA/C	Skip if not interrupting	Receive Control Register 1	Receive Control Register 1
05	Set transmit interrupt mask	Skip if transmit not interrupting	Receive Control Register 2	Receive Control Register 2
06	Set transmit DMA/C	Skip if ready to transmit	Transmit Control Register 1	Transmit Control Register 1
07	Reset transmit interrupt mask and DMA/C	Skip if ready to receive	Transmit Control Register 2	Transmit Control Register 2
10	Enable Input & Output and Set full-duplex mode	Skip if not Search for Sync	Input Character to A	
11	Diagnostic sync	Skip if Input* Bit 1 Marking	Input ID	
12	Enable Input + Output mode Reset full-duplex + Diagnostic mode	Skip if Input Bit 2 Marking		
13	Set Diagnostic mode	Skip if Input Bit 3 Marking		

Op Code / Fctn Code	OCP	SKS	INA	OTA
14	Search for Sync	Skip if Input Bit 4 Marking	Receive DMA/C	Receive DMA/C Channel Address
15	Set Interrupt Mask	Skip if Parity Error	Transmit DMA/C	Transmit DMA/C Channel Address
16	Reset Interrupt Mask	Skip if Overrun Error	Receive Interrupt Vector	Receive Interrupt Vector
17	Initial	Skip if Framing Error	Transmit Interrupt Vector	Transmit Interrupt Vector

*OPEN = MARK = -12
SPACE = +12

5.1.2.1 BPIOC as PTR

Device Address = '01
ID = '101

Op Code / Fctn Code	OCP	SKS	INA	OTA
00	Start	Skip if Ready	Input Data Register + "OR" with A	
01	Stop	Skip if Power On		
02	Forward	Skip if Right Byte Next		
03	Reverse			
04		Skip if Not Interrupting		
05				
06				
07				
10			Input Data Register to A	Control Register
11			Input ID	
12				
13				
14	Enable DMA/C		DMA/C Channel Address	DMA/C Channel Address
15	Set Interrupt Mask			
16	Reset Interrupt Mask		Interrupt Vector	Interrupt Vector
17	Initialize			

5.1.2.2 BPIOC as PTP

Device Address = '02
ID = '102

Op Code / Fctn Code	OCP	SKS	INA	OTA
00	Start	Skip if Ready		Output Data Register
01	Stop	Skip if Power On		
02		Skip if Right Byte Next		
03				
04		Skip if Not Interrupting		
05				
06				
07				
10				Control Register
11			Input ID	
12				
13				
14	Enable DMA/C		DMA/C Channel Address	DMA/C Channel Address
15	Set Interrupt Mask			
16	Reset Interrupt Mask		Interrupt Vector	Interrupt Vector
17	Initialize			

5.1.2 BPIOC

Device Address = '30 '31
ID = '101 '102

Fctn Code \ Op Code	OCP	SKS	INA	OTA
00	Start	Skip if Ready	Input Data Register + "OR" with A	Output Data Register
01	Stop	Skip if Device Status		
02	Forward	Skip if Right Byte Next		
03	Reverse			
04		Skip if Not Interrupting		
05				
06				
07				
10			Input Data Register to A	Control Register
11			Input ID	
12				
13				
14	Enable DMA/C		DMA/C Channel Address	DMA/C Channel Address
15	Set Interrupt Mask			
16	Reset Interrupt Mask		Interrupt Vector	Interrupt Vector
17	Initialize			

5.1.3 LFC, PIC and WDT

Device Address = '20
ID = '120

Fctn Code \ Op Code	OCP	SKS	INA	OTA
00	Start	Skip if Not Interrupting		
01	Acknowledge PIC Interrupts			
02	Stop	Skip if Not Memory Increment Overflow	Input PIC Register	Load PIC Register
03				
04	Select Line Frequency			
05	Select External Clock	Skip if WDT Time-out		
06	Start WDT			
07	Stop WDT	Skip if WDT caused SYSCL-		Load Control Register
10				
11			Input ID	
12			Memory Increment Cell Number	Memory Increment Cell Number
13			Interrupt Vector	Interrupt Vector
14				
15	Set Interrupt Mask			
16	Reset Interrupt Mask			
17	Initialize			

5.2 Control Register Summary

5.2.1 ASLC and SSLC

5.2.1.1 Receive Control Register 1

Bit	Interpretation
1	Control Bit Port 1
2	Control Bit Port 2
3	Receive Port Select
4	
5	Clock Speed (N)
6	
7	
8	
9	$N = 4096 \times \frac{16}{5} \times 16 \times 10^{-6} \times \text{Baud}$ (for Async)
10	$N = 4096 \times \frac{16}{5} \times 10^{-6} \times \text{Baud}$ (for Sync)
11	
12	
13	
14	
15	
16	

Baud	N	Baud	N
75	'17	1200	'373
110	'27	2400	'767
150	'37	4800	'1756
300	'76	9600	'3735
600	'175	19200	'7672

5.2.1.2 Receive Control Register 2

Bit	Interpretation
1	Select Synchronous Receive (SSLC only)
2	Number of Stop Bits — 0 = 1 stop; 1 = 2 stop (1.5 for 5-bit)
3	Character Length — 00 = 5 bits; 10 = 6 bits; 01 = 7 bits; 11 = 8 bits
4	
5	Parity Inhibit — 0 = enable parity check; 1 = disable parity check
6	Select Even Parity — 0 = odd; 1 = even
7	0
8	0
9	Sync Character (SSLC only)
10	
11	
12	
13	
14	
15	
16	

5.2.1.3 Transmit Control Register 1

Bit	Interpretation
1	Control Bit Port 3
2	Control Bit Port 4
3	Transmit Port Select
4	
5	Clock Speed (N) (see 5.2.1.1)
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	

5.2.1.4 Transmit Control Register 2

Bit	Interpretation	
1	Select Synchronous Transmit (SSLC only)	
2	Number of Stop Bits	0 = 1 stop 1 = 2 stop (1.5 for 5-bit)
3	Character Length	00 = 5 bits 10 = 6 bits 01 = 7 bits 11 = 8 bits
4		
5	Parity Enable	0 = enable parity generate 1 = disable parity generate
6	Select Even Parity	0 = odd 1 = even
7	0	
8	0	
9	Fill character for idle line (SSLC only)	
10		
11		
12		
13		
14		
15		
16		

5.2.2.1 BPIOC as PTR

Bit	Interpretation
1	0
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	0
14	Enable Byte-Packing
15	0
16	0

5.2.2.2 BPIOC as PTP

Bit	Interpretation
1	0
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	0
14	Enable Byte-Packing
15	0
16	0

5.2.2.3 BPIOC

Bit	Interpretation
1	0
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	Set to Output Mode
14	Enable Byte-Packing
15	Set Independent Reverse Flag
16	Set Device Enable Flag

5.2.3 LFC, PIC, WDT

Bit	Interpretation
1	0
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	Enable PIC to generate MI (Memory Increment)
12	Set PIC clock to 102.4 usec
13	Enable MI overflow to generate interrupt
14	Enable PIC to generate interrupt
15	Start PIC
16	Enable WDT timeout to generate system reset

TABLE 3-1. EIA Serial Device Connections(Connector C)

NAME	CONN PIN
EIAC4+	CC-1 - EIA Control Output Bit 4
GND	CC-2
EIAC3+	CC-3 - EIA Control Output Bit 3
GND	CC-4
EIAC3+	CC-5 - EIA Control Output Bit 3
GND	CC-6
EIAC2+	CC-7 - EIA Control Output Bit 2
GND	CC-8
EIAC1+	CC-9 - EIA Control Output Bit 1
GND	CC-10
TXEIA3-	CC-11 - EIA Transmit Output Bit 3
GND	CC-12
TXEIA4-	CC-13 - EIA Transmit Output Bit 4
GND	CC-14
TXEIA1-	CC-15 - EIA Transmit Output Bit 1
GND	CC-16
TXEIA2-	CC-17 - EIA Transmit Output Bit 2
GND	CC-18
EIAC1+	CC-19 - EIA Control Otuput Bit 1
GND	CC-20
INBIT3-	CC-21 - EIA Control Input Bit 3
GND	CC-22
INBIT4-	CC-23 - EIA Control Input Bit 4
GND	CC-24
INBIT3-	CC-25 - EIA Control Input Bit 3
GND	CC-26
INBIT2-	CC-27 - EIA Control Input Bit 2
GND	CC-28
INBIT1-	CC-29 - EIA Control Input Bit 1
GND	CC-30
INBIT1-	CC-31 - EIA Control Input Bit 1
GND	CC-32
RXEIA1+	CC-33 - EIA Receive Input Bit 1
GND	CC-34
RXEIA2+	CC-35 - EIA Receive Input Bit 2
GND	CC-36
PREXCL+	CC-37 - Synchronous Clock Receive Input (EIA)
GND	CC-38
RXEIA3+	CC-39 - EIA Receive Input Bit 3
GND	CC-40
RXEIA4+	CC-41 - EIA Receive Input Bit 4
GND	CC-42
PTEXCL+	CC-43 - Synchronous Clock Transmit Input (EIA)
GND	CC-44

TABLE 3-2. Current Loop Serial Device and Clock Connection (Connector D)

NAME	CONN PIN	
RXEIA1+	CD-1	┐ Connect Together for Current Loop Operation on
GND	CD-2	├ Channel 1
CLIN+	CD-3	┘
	CD-4	
CLIN+	CD-5	- Current Loop Input +
	CD-6	
CLIN-	CD-7	- Current Loop Input -
	CD-8	
TXCL2-	CD-9	- Current Loop Transmit Output, Channel 2
	CD-10	
TXCL1-	CD-11	- Current Loop Transmit Output, Channel 1
	CD-12	
TXCL3-	CD-13	- Current Loop Transmit Output, Channel 3
	CD-14	
TXCL4-	CD-15	- Current Loop Transmit Output, Channel 4
	CD-16	
	CD-17	
	CD-18	
TXCLR2+	CD-19	- Current Loop Transmit Return, Channel 2
	CD-20	
TXCLR1+	CD-21	- Current Loop Transmit Return, Channel 1
	CD-22	
TXCLR3+	CD-23	- Current Loop Transmit Return, Channel 3
	CD-24	
TXCLR4+	CD-25	- Current Loop Transmit Return, Channel 4
	CD-26	
	CD-27	
	CD-28	
	CD-29	
	CD-30	
EXTCLK+	CD-31	- LFC External Clock Input, TTL Levels
GND	CD-32	
SCOPESY	CD-33	┐
	CD-34	├ For Diagnostic Use Only. Do Not Connect.
WDTTST	CD-35	┘
	CD-36	
WDTEXS-	CD-37	┐
	CD-38	├ WDT External Contact Output
RETOUT-	CD-39	┘
	CD-40	
EXPFI-	CD-41	┐
	CD-42	├ WDT External System Clear Input
RETIN-	CD-43	┘
	CD-44	

LTR	DATE	REVISION	DR.	CK.

TABLE 3-3. Buffered Parallel I/O Channel No. 2 External Connections (Connector E)

NAME	CONN PIN	
B20D01_	CE-1	- A Reg Bit 9
GND	CE-2	
B20D02+	CE-3	- A Reg Bit 10
GND	CE-4	
B20D03+	CE-5	- A Reg Bit 11
GND	CE-6	
B20D04+	CE-7	- A Reg Bit 12
GND	CE-8	
B20D05+	CE-9	- A Reg Bit 13
GND	CE-10	
B20D06+	CE-11	- A Reg Bit 14
GND	CE-12	
B20D07+	CE-13	- A Reg Bit 15
GND	CE-14	
B20D08+	CE-15	- A Reg Bit 16
GND	CE-16	
B20D09+	CE-17	- A Reg Bit 1
GND	CE-18	
B20D10+	CE-19	- A Reg Bit 2
GND	CE-20	
B20D11+	CE-21	- A Reg Bit 3
GND	CE-22	
B20D12+	CE-23	- A Reg Bit 4
GND	CE-24	
B20D13+	CE-25	- A Reg Bit 5
GND	CE-26	
B20D14+	CE-27	- A Reg Bit 6
GND	CE-28	
B20D15+	CE-29	- A Reg Bit 7
GND	CE-30	
B20D16+	CE-31	- A Reg Bit 8
GND	CE-32	
D2SKS	CE-33	- Device Status Input
GND	CE-34	
D2MVF	CE-35	- Forward Data Strobe Output
GND	CE-36	
D2RDY	CE-37	- Device Ready Input
GND	CE-38	
D20TA	CE-39	- Device Enable Output
GND	CE-40	
D2STRB	CE-41	- Device Data Strobe Input
GND	CE-42	
D2MVR	CE-43	- Reverse Data Strobe Output
GND	CE-44	

Word Mode: Right Byte
Byte Mode: Connect here. Left byte is transmitted first.

Word Mode: Left Byte
Byte Mode: Not Used

USED ON	SCALE	SIZE	DWG. NO.	REV.
NEXT ASSY	SHEET 45 OF 48		SPC 1831	

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LTR	DATE	REVISION	DR.	CK.

TABLE 3-4. Buffered Parallel I/O Channel No. 1 External Connections (Connector F)

NAME	CONN PIN	
B10D01+	CF-1	- A Reg Bit 9
GND	CF-2	
B10D02+	CF-3	- A Reg Bit 10
GND	CF-4	
B10D03+	CF-5	- A Reg Bit 11
GND	CF-6	
B10D04+	CF-7	- A Reg Bit 12
GND	CF-8	
B10D05+	CF-9	- A Reg Bit 13
GND	CF-10	
B10D06+	CF-11	- A Reg Bit 14
GND	CF-12	
B10D07+	CF-13	- A Reg Bit 15
GND	CF-14	
B10D08+	CF-15	- A Reg Bit 16
GND	CF-16	
B10D09+	CF-17	- A Reg Bit 1
GND	CF-18	
B10D10+	CF-19	- A Reg Bit 2
GND	CF-20	
B10D11+	CF-21	- A Reg Bit 3
GND	CF-22	
B10D12+	CF-23	- A Reg Bit 4
GND	CF-24	
B10D13+	CF-25	- A Reg Bit 5
GND	CF-26	
B10D14+	CF-27	- A Reg Bit 6
GND	CF-28	
B10D15+	CF-29	- A Reg Bit 7
GND	CF-30	
B10D16+	CF-31	- A Reg Bit 8
GND	CF-32	
DISKS	CF-33	- Device Status Input
GND	CF-34	
D1MVF	CF-35	- Forward Data Strobe Output
GND	CF-36	
D1RDY	CF-37	- Device Ready Input
GND	CF-38	
D10TA	CF-39	- Device Enable Output
GND	CF-40	
D1STRB	CF-41	- Device Data Strobe Input
GND	CF-42	
B1MVR	CF-43	- Device Data Strobe Output
GND	CF-44	

Word Mode: Right Byte
Byte Mode: Connect here. Left byte is transmitted first.

Word Mode: Left Byte
Byte Mode: Not Used

USED ON	SCALE	SIZE	DWG. NO.	REV.
NEXT ASSY	SHEET 46 OF 48		SPC 1831	

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APPENDIX A

With 100' of Belden type 8445/8456 cable there will be no more than 2% distortion at 19.2 KB

With 10' of Belden type 8445/8456 cable there will be no more than 2% distortion at 50 KB

These are computed as follows:

distortion = [(cable length (ft) X capacitance (pf/ft) + 330pf) X 400 ohm (effective impedence) X 10^{-6}] X 100 /[1 bit time (in usec)]

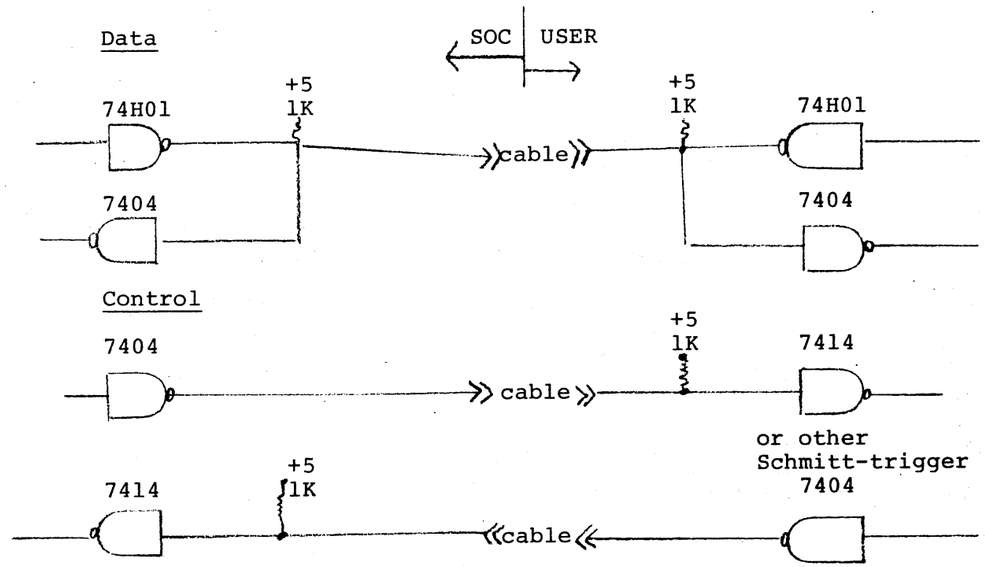
e.g. Belden type 8445 (5 conductor) cable is 20 pf/ft

distortion = 100'X 20 X 400 X 10^{-6} X 100/50
= 80/50
= 1.6%

Driver is EIA 1488 with 330 pf slew control.

Receiver is EIA 1489.

APPENDIX B



cable: #24 to #28 twisted pair

10' cable 200 ns settle time

25' cable 500 ns settle time

100' cable 2 us settle time

DATE: March 1, 1976

TO: Programming and Engineering

FROM: Richard Lupo

SUBJECT: GOULD-VERSATEC-SOC PRODUCT SPECIFICATION

1.0 This document describes the PRIME Gould-Versatec printer/ plotter controller and its programming requirements.

2.0 General Description (Controller)

The controller is a subset of the PRIME System Option Controller (SOC) board. It utilizes the buffered parallel in/ out channels (BPIOC 1&2) of the SOC to transfer data, status, and control information to the Gould or Versatec device.

2.1 Operation (Ref. PRIME Manual Man 1944)

a). BPIOC1 is utilized to transfer data to the device buffer in both word and byte mode. With each data transfer, a clock pulse is generated to signal the device that data is present on its input lines. The device responds by requesting subsequent data (word or byte) via its data request line. Data is always transmitted from bits 1-8 of BPIOC1 regardless of data mode. If word mode is current, BPIOC1 data bits 9-16 are swapped with data bits 1-8, then the device is alerted to the data present at its input lines. When the transfer is complete, the device requests additional data which sets the BPIOC1 READY making it ready to accept subsequent data transfers. If byte mode is current, data is first transmitted from BPIOC1 data bits 1-8. When the device responds with a request for additional data, the data in bits 9-16 are swapped with bits 1-8 and then transmitted to the device. When the device responds to the second byte, the BPIOC1 READY is set making BPIOC1 ready to accept subsequent data transfers.

b). BPIOC2 is utilized to issue function commands to the device and input device status.

2.2 Status

Device status is present on BPIOC2 bits 9-12. When an input BPIOC2 command (INA) is issued, the data is swapped into BPIOC2 bits 1-4, then transmitted to the processor A register bits 1-4. Versatec status is defined

in Appendix A and Gould status is defined in Appendix B.

2.3 Function Commands

Each device has a set of function commands to initiate character imaging and paper movement functions. The specific command sets are specified in Appendix A (Versatec) or Appendix B (Gould).

2.4 Data Transfer - Data can be transferred to the system option controller utilizing programmed in/out mode (PIO), direct memory access mode (DMA) or direct memory channel mode (DMC). BPIOC1 is normally set to DMA mode for data transfers to the device and BPIOC2 is always set to PIO mode.

3.0 Programming Specification

Specific programming instructions for each SOC-device interface appear in Appendix A (Versatec) or B (Gould). With the exception of special programming sequences for each device interface, the programming of the BPIOC's (1&2) is as specified in PRIME Manual Man 1944. These exceptions are due to the lack of device response to status input instructions (INA) and the need for special handling of the issuance of certain command functions. To overcome these constraints, the instruction sequences specified in the applicable appendix (A or B) must be executed.

Appendix A

This Appendix describes the Versatec-Soc function commands, instruction set and programming requirements.

Contents: Section 1 Versatec Function Command Description
Section 2 Versatec-Soc Instruction Set Description
Section 3 Programming Sequences

1.0 Function Commands

Function commands can be transmitted to the device via BPIOC2 bits 13-16, or, in the case of devices with a 64 or 96 character ASCII printing set, they can be included in the data stream (print mode only). The device simultaneous print-plot control line is controlled by BPIOC2 control register bit 16. BPIOC2 is also utilized to determine if the device is returning a device ready status via the D2SKS status line.

The device requires that it be in a defined state prior to the execution of its command set. Therefore, the Ready status of the device must be tested prior to issuing commands.

Command Completion
The Versatec device responds to data and function commands via the device Ready line. Upon receipt of a function command or data, the device Ready returns a Not Ready (Busy) status. This status will return to the Ready state when the device is ready to accept new data or has successfully completed a paper motion or control command. This response can be sensed by testing the device Ready line, by testing the BPIOC1 Ready, which sets as a result of the device ready line's transition from Not Ready to Ready, or by enabling the BPIOC1 interrupt logic, which will result in an interrupt request when BPIOC1 Ready is set as in the previous case.

1.1 ASCII Function Codes (via BPIOC1 Data Register)

1	004	End of Transmission
2	014	Form Feed
3	012	Line Feed
4	015	Carriage Return

1.2 Code Descriptions

1.2.1 1 End of Transmission (EOTR):
Causes print cycle and paper advance of 8 inches, then stop if in roll mode, or continue advance to top of next page if in fan-fold mode. Do not use if in SPP mode.

1.2.2 2 Form Feed (FE):
Causes print cycle and paper advance of 2½ inches if in roll mode, or advance to top of next page if in fan-fold mode. Do not use if in SPP mode.

1.2.3 3 Line Feed (LF):
Causes print cycle and paper advance of one line except when- (a) Follows printing a full buffer. (b) Follows a Carriage Return which causes a print cycle.

1.2.4 4 Carriage Return (CR):
Causes print cycle and paper advance of one line, only if buffer has at least one character entered but is not full.

1.3 Function Commands (via BPIOC2 Data Register)

BPIOC2 Bits	13	14	15	16	
	0	0	0	1	Issue End of Transmission
	0	0	1	0	Issue Device Reset
	0	1	0	0	Issue Form Feed
	1	0	0	0	Issue Device Clear

Note: In NO case are control codes to be issued simultaneously.

1.4 Command Descriptions

1.4.1 End of Transmission (EOTR)
A. Forces Write Cycle
B. With Fan-Fold Operation causes paper to advance 8 inches then to top of next page.
C. With Roll Operation causes paper to advance approximately 8 inches.

1.4.2 Device Reset (RESET)
Clears the device data buffer and resets control logic.

1.4.3 Form Feed (FF)
A. Forces Write Cycle.
B. With Fan-Fold Operation causes paper to advance to top of next page.
C. With Roll Operation causes paper to advance approximately 2.5 inches.
D. Do not use when in the print phase of simultaneous print/plot mode.

1.4.4 Device Clear(CLEAR)
Clears the device data register.

1.5 Function Commands (via BPIOC2 Control Register)

BPIOC2 Control Register Bit	16	
	0	SPP Disabled
	1	SPP Enabled

1.5.1 Command Description

SPP Disabled
Inhibits simultaneous printing and plotting of data.

SPP Enabled
Allows simultaneous printing and plotting of data when used in conjunction with the print/plot command as described in section 2.2b of this document.

2.0 VERSATEC SOC INSTRUCTION SET DESCRIPTION
The Versatec-Soc address of BPIOC1 is '33. The address of BPIOC2 is '34.

2.1 OCP Instructions

2.1.1 OCP '0033, '0034

Start. This enables the BPIOC to transfer data, resets the data register, and resets the right-byte-next flag.

2.1.2 OCP '0133, '0134

Stop. This prevents further data transfer. The BPIOC must be stopped prior to a direction switch and prior to a control register change.

2.1.3 OCP '0233, '0234

Forward. This sets the forward/reverse flop. Issuing this command has the following results.

BPIOC1 - Enables data clocks to be sent to the device (PICLK).

BPIOC2 - Enables BPIOC2 Ready to be set automatically after having been reset due to an output function command (OTA).

2.1.4 OCP '0333, '0334

Reverse. This resets the forward/reverse flop. Issuing this command has the following results.

BPIOC1 - Disables data clocks to the device.

BPIOC2 - Disables the automatic setting of BPIOC2 Ready.

2.1.5 OCP '1433

DMA/C. This enables BPIOC1's DMA/C mode.

2.1.6 OCP '1533, '1534

Set Interrupt Mask.

2.1.7 OCP '1633, '1634

Reset Interrupt Mask.

2.1.8 OCP '1733, '1734

Initialize. This sets Stop and Forward. This resets the data register, right-byte-next, Interrupt Mask, DMA/C enable, and the control register (initial of Input/Output) non Byte-pack, reset Independent Reverse and reset Device Enable.

2.2 SKS INSTRUCTIONS

2.2.1 SKS '0033, '0034

Skip if BPIOC is ready for data transfer.

2.2.2 SKS '0133

Skip if device is on-line (power on).

2.2.3 SKS '134

Skip if device ready (power on, not busy moving paper or printing).

2.2.4 SKS '0433, '0434

Skip if BPIOC not interrupting. The BPIOC will request an interrupt, if it is ready, in PIO (non-DMA/C) mode and has its mask set.

2.3 INA INSTRUCTIONS

2.3.1 INA '34

Input device status if ready and input mode and "OR" with A. The INA resets ready.

2.3.2 INA '1034

Same as INA '0034 except that A is cleared prior to the operation. The status word returned is interpreted as follows:

Bit	1	2	3	4	5——16
1		Off-line	Not Ready	No Paper	Not Used
0	Versatec	On-line	Ready		

Bit 1 always returns a "0" if a versatec device is attached to the controller.

Bit 2 defines the setting of the device on/off switch.

Bit 3 (if a "1") indicates the device is not ready, e.g., busy printing/plotting, moving paper or off-line.

Bit 4 (if a "1") indicates the device paper supply has been depleted.

2.3.3 INA '1133, '1134

Input ID. The ID of BPIOC(1) is ('101). The ID of BPIOC(2) is ('102).

2.3.4 INA '1433

Input DMA/C channel address.

2.3.5 INA '1633, '1634

Input interrupt vector.

2.4 OTA INSTRUCTIONS

2.4.1 OTA '0033, '0034

Output A to BPIOC data register if ready and output mode. The OTA resets BPIOC Ready.

2.4.2 OTA '1033, '1034

Output A to Control Register.

Versatec Device

BPIOC1 control register:

	Bit 13	Bit 14	Bit 15	Bit 16
1	Not used	Set to byte mode	———	Plot mode
0	Set to output mode	Set to word mode	———	Print mode

BPIOC2 control register:

	Bit 13	Bit 14	Bit 15	Bit 16
1	Set to input mode	Set to byte mode	———	Simultaneous Print-Plot
0	Set to output mode	Set to word mode	———	———

2.4.3 OTA '1433

Output DMA/C channel address. The format is as follows:

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5←→Bit 16
1	Input Transfer	———	1	DMC mode	Channel Address
0	Output Transfer	0	———	DMA mode	

2.4.4 OTA '1633,'1634

Output interrupt vector. The format is as follows:

	Bit 1←→Bit 4				Bit 5←→Bit 16
1	-	-	-	-	Interrupt Vector
0	0	0	0	0	

3.0 PROGRAMMING SEQUENCES

3.1 Device Status

Executing the following sequence will input the device status.

INA Device Status:

```
SB     BSS   1          Status Bin
STAT   DAC   **         Subr Entry Point
       OCP   '133       Disable BPIOC1 Operation
       OCP   '134       Disable BPIOC2 Operation
       OCP   '234       Set BPIOC2 to Forward Mode
                          (Enable Forward Data Strobe)
       LDA   ='14       Set BPIOC2 to Input Mode &
                          Byte Mode & Independent
       OTA   '1034        Forward Mode & Print Mode
       HLT   (or Error Exit)
       OCP   '34        Enable BPIOC2 Operation
       INA   '1034      Clear A and Read Device Status
                          Lines into A (via BPIOC2 data
       HLT   (or Error Exit)                  Register)
       STA   SB         Save Device Status
       JMP*  STAT       Exit
```

3.2 Function Commands

Each device requires a set of explicit function (control) commands for device control, paper motion and data printing. To properly issue these commands the following instructions sequences must be executed:

3.2.1 Paper Motion and Print Commands

Prior to issuing the "Home", "Feed" or "Print Line" Command, the device "Busy" must be tested and verified false. When the device is issued a paper motion command, i.e., Feed or Home, it responds at the completion of paper motion to BPIOC1*. This response will set BPIOC1 Ready. (See paragraph 1.0.) The setting of BPIOC2 Ready will cause an interrupt request if the BPIOC2 interrupt mask has been set. If the device is operated in an interrupt inhibited environment, completion can be tested with a skip if BPIOC1 is not interrupting or skip if BPIOC1 is ready instruction.

*via the device Ready Line

3.2.2 Device Control and Paper Motion Commands

BPIOC2 is used to issue control and paper motion commands to the Versatec device. BPIOC1 is utilized to inform the program of command completion in an interrupt enabled environment. The Versatec device will also respond to ASCII control codes in the data stream. The specific modes of issuing these ASCII Codes are covered in paragraph 1.1.

The paper motion and control sequence is as follows: (Note that this does not include the case of ASCII Control characters in the data stream.)

```
PMC    BSS   1          Command Bin
PMS    DAC   **         Subr Entry Point
       SKS   '134       Test for Versatec Ready
       JMP   *-1        Wait or Error Exit
       OCP   '133       Disable BPIOC1 Operation
       OCP   '134       Disable BPIOC2 Operation
       OCP   '1533      Set BPIOC1 Interrupt Mask
                          (required if interrupt enabled)
       OCP   '33        Enable BPIOC1 Operation
       OCP   '234       Set BPIOC2 to Enable Forward
                          Data Strobe
       LDA   ='0        Clear A
       OTA   '1034      Set BPIOC2 to Output Mode &
       JMP   *-1          Word Mode & Independent Word
                          Mode & Print Mode
       OCP   '34        Enable BPIOC2 Operation
       LDA   PMC        Get Command From Bin
       OTA   '34        Issue Command
       HLT   (or Error Exit)

Case 1: JMP*  PMS       Exit if Interrupts Enabled

With Interrupts Disabled:

Case 2: SKS   '134      Test Device Ready Line
        JMP    Case 2   Wait for Device Ready
        JMP*   PMS      Exit

Case 3: SKS   '33       Test BPIOC1 Ready
        JMP    Case 3   Wait for Device Response to
                          set BPIOC1 Ready
        JMP*   PMS      Exit

Case 4: SKS   '433      Test BPIOC1 Interrupt Request
                          Logic
        JMP*   PMS      Exit when Device Response has
                          Set BPIOC2 Ready which will
                          result in an Interrupt Request
                          if the Mask is Set
        JMP    Case 3   Wait for Device Response
```

3.2.3 Print Line Command

BPIOC1 is used to issue a print line command to the device. This command causes the device to print the current contents of its print or plot buffer and advance the paper one line (one scan line if plot mode, one character scan if print mode.)

The print line sequence is as follows:

```
PLS     DAC  **              Subr Entry
        OCP  '133            Disable BPIOC1 Operation
        OCP  '1533           Set BPIOC1 Interrupt Mask
                               (required if interrupts enabled)
        OCP  '333            Inhibit Data Clock (disable
                               forward data strobe)
        LDA  ='2             Set BPIOC1 to Independent
        OTA  '1033           Reverse Mode (Enable Independent
        HLT  (or Error Exit)   Reverse Strobe) & Output Mode
                               & Word Mode & Print Mode
        OCP  '33             Enable PBIOC1 Operation
        OTA  '33             Issue Command
        HLT  (or Error Exit)

Case 1: JMP* PLS             Exit if Interrupts Enabled

Case 2: SKS  '134            Test Device Ready Line
        JMP  Case 2          Wait for Device Ready
        JMP* PLS             Exit
Case 3: SKS  '33             Test BPIOC1 Ready
        JMP  Case 3          Wait for Device Response
        JMP* PLS               to Set BPIOC1 Ready

Case 4: SKS  '433            Test BPIOC1 Interrupt Request
                               Logic
        JMP* PLS             Exit when Device Response has
                               Set BPIOC1 Ready which will
                               result in an Interrupt Request
                               if the Mask is Set
        JMP  Case 4          Wait for Device Response
```

3.2.4 Simultaneous Print/Plot

The one remaining control mode for the Versatec Device is Simultaneous Print/Plot mode. In this mode the device will accept data destined for its print and plot buffers prior to imaging the data on paper. To successfully complete this sequence, data must be presented until the device print buffer is full or a line terminating character has been received (print line or ASCII 215). At that point, the device will become Not Ready (Busy) until the operating mode is changed from print to plot. Changing modes signals the device to return a Ready (Not Busy) status and to accept plot data until the buffer is full or a line terminating character (Print Line Only) has been received. Upon receipt of the print line or buffer full, the device will image one plot scan line of data. It should be noted that the alpha data (print) requires (depending on Versatec Device) between eight to twenty lines of scan data to image a complete character. Therefore, the print mode of

simultaneous print/plot (SPP) should not be re-entered until the alpha characters have been scanned. Another constraint of SPP mode is that the issuing of REOTR or RFFED or the ASCII code for End of Transmission (ASCII 004) or Form Feed (ASCII 014) are not valid when the print phase of SPP mode is current. In plot mode the REOTR signal will be accepted by the device. It must be stressed that the simulataneous print/plot mode requires completion of both phases of this mode and the proper data and control sequences (print then plot) must be adhered to for successful completion.

3.3 Data Transfers

Data transfers take place via BPIOC1. These transfers can be implemented in programmed input-output (PI/O) mode or direct memory access (DMA/C) mode with interrupts enabled or disabled. In all cases BPIOC1 must be set to output mode, with byte or word mode selected, independent reverse data strobe disabled, forward data strobe enabled and print or plot mode selected.

The following sequences are examples of existing instructions used in test programs.

3.3.1 Versatec Device (Not Simultaneous Print/Plot) PI/O Mode Data Transfer (Interrupts Disabled)

Case 1: Output a block of data.

```
VPIO    DAC  **              Subr Entry
        OCP  '133            Disable BPIOC1 Operation
        OCP  '233            Enable Data Clock (Enable Forward
                               Data Strobe)
        OCP  '33             Enable BPIOC1 Operation
        LDA ='4/'1           Set BPIOC1 to Output Mode & Byte Mode
                               & Independent Forward Mode &
                               Print Mode/Plot Mode
                  -or-
        LDA ='1/'4           Set BPIOC1 to Output Mode & Word
                               Mode & Independent Forward Mode
                               & Plot Mode/Print Mode
        OTA  '1033
        HLT  (or Error Exit)

        LDA  VPIOP           Set up Data Pointer and Word Count
        STA  OP
        LDA  VPIOC
        STA  OC
PIOD1   LDA* OP              Get Data Word
        OTA  '33             Send it, if BPIOC1 is Ready
        JMP  *-1             BPIOC1 Not Ready.  Wait for Device
                               Ready to Set BPIOC1 Ready
        IRS  OP              Increment Pointer
        IRS  OC              Decrement Count
        JMP  PIOD1           Continue
        JMP* PIOD            Exit
```

3.3.2 Versatec Device (Not Simultaneous Print/Plot) PI/O Mode Data Transfer (Interrupts Enabled)

Case 2: Output a word of data.

```
VPIO    DAC  **              Subr Entry
        OCP  '133            Disable BPIOC1 Operation
        OCP  '233            Enable Data Clock (Enable Forward
                               Data Strobe
```



```
        OCP  '1533           Set BPIOC1 Interrupt Mask
        OCP  '33             Enable BPIOC1 Operation
        LDA ='4/'1           Set BPIOC1 to Output Mode & Byte Mode
                               & Independent Forward Mode &
                               Print Mode/Plot Mode
                  -or-
        LDA ='1/'4           Set BPIOC1 to Output Mode & Word
                               Mode & Independent Forward Mode
                               & Plot Mode/Print Mode
        OTA  '1033
        HLT  (or Error Exit)
        LDA   Data Word      Get Data Word
        OTA  '33             Send it
        HLT  (or Error Exit)
        ENB                  Enable Interrupts
        JMP* PIOD            Exit and Wait for Device Ready to Set
                               BPIOC1 Ready which will result in
                               a BPIOC1 interrupt request.
```

Versatec Device (Not Simultaneous Print/Plot)
DMA Mode Data Transfer (With Interrupts Enabled)

```
VDMA    DAC  **              Subr Entry
        OCP  '133            Disable BPIOC1 Operation
        OCP  '233            Enable Data Clock (Enable Forward
                               Data Strobe)
        OCP  '1433           Set BPIOC1 to DMA/C Mode
        OCP  '1533           Set BPIOC1 Interrupt Mask
        LDA ='4/'1           Set BPIOC1 to Output Mode & Byte Mode
                               & Independent Forward Mode &
                               Print Mode/Plot Mode
                  -or-
        LDA ='1/'4           Set BPIOC1 to Output Mode & Word Mode
                               & Independent Forward Mode &
                               Plot Mode/Print Mode
        OTA  '1033
        HLT  (or Error Exit)
        LDA  ='200XX         Set BPIOC1 to DMA & Output Mode where
                               XX is the Even Address of an Even
                               Odd Channel Pair in Register File
                               (Addresses 20_8 to 37_8)
        OTA  '1433
        HLT  (or Error Exit)
        LDA  =VINTHP         Set up Interrupt Vector Address
        OTA  '1633
        HLT  (or Error Exit)
        LDA  VDMAC           Set DMA Word Count, using Channel
                               Pair 20 and 21
        STA  '20
        LDA  VDMAP           Set Beginning Address
        STA  '21
        OCP  '33             Start DMA Transfers
        ENB                  Enable Interrupts
        JMP* DMAD            Exit and wait for DMA End of Range to
                               set BPIOC1 Interrupt Reguest
```

Versatec Device (Not Simultaneous Print/Plot)

3.3.4 DMC Mode Data Transfer (with Interrupts Enabled)

```
VDMC    DAC  **              Subr Entry
        OCP  '33            Disable BPIOC1 Operation
        OCP  '233           Enable Data Clock (Enable Forward
                              Data Strobe)
        OCP  '1433          Set BPIOC1 to DMA/C Mode
        OCP  '1533          Set BPIOC1 Interrupt Mask
        LDA ='4/'1          Set BPIOC1 to Output Mode & Byte
                              Mode & Independent Forward Mode
                              & Print Mode /Plot Mode
                    -or-
        LDA ='1/'4          Set BPIOC1 to Output Mode & Word
                              Mode & Independent Forward Mode &
                              Plot Mode/Print Mode
        OTA  '1033
        HLT  (or Error Exit)
        LDA  ='3XXXX        Set BPIOC1 to DMC Mode where XXXX is
                              the Even Address of an Even Odd
                              Channel Pair, in memory, which
                              contains the beginning address of
                              the data to be transferred followed
                              by the ending address of the data
                              to be transferred in the odd address.
        OTA  '1433
        HLT  (or Error Exit)
        OCP  '33            Enable BPIOC1 Operation
        ENB                 Enable Interrupts
        JMP* VDMC           Exit and wait for DMC End of Range
                              to set BPIOC1 Interrupt Request
```


APPENDIX B

This appendix describes the Gould-SOC function commands, instruction set and programming requirements. Contents:

Section 1 Gould Function Command Description
Section 2 Gould-SOC Instruction Set Description
Section 3 Programming Sequences

1.0 Gould Function Commands

Function commands are transmitted to the device via BPIOC2 bits 5-8 after having been loaded into and swapped from BPIOC2 bits 13-16. A device reset command is also transmitted via BPIOC2 control register. This is accomplished by setting and then clearing BPIOC2 control register bit 16. BPIOC2 is also utilized to determine if the device is returning a device selected (SELECT) status via the D2SKS status line.

1.1 Gould Function Command Set

BPIOC2

Bits	13	14	15	16	
	0	0	0	0	Feed roll paper 128 steps Feed fan fold paper to top of form
	0	0	0	1	Set to graphic (plot) mode
	0	0	1	0	(optional) Cut paper
	0	0	1	1	Printer enable
	0	1	0	0	Printer disable and set alpha mode
	0	1	0	1	Last line flag set
	0	1	1	0	Not used
	0	1	1	1	Not used
	1	0	0	0	Home (feed roll/fan fold paper 256 steps)
	1	0	0	1	Issue print line command

1.2 Command Descriptions

1.2.1 Feed Command:

This command requires that the printer is enabled and not "busy". The paper is fed 128 raster steps on roll equipped

units. The paper is fed to top-of-form on fan-fold equipped units. "Busy" status is reported until the operation completes.

1.2.2 Graphic Select:

This command requires that the printer is disabled. The "alpha/graphic" mode control to the printer is set to "graphic". The command is immediate and does not interrupt.

1.2.3 Cut Paper:

This command requires the printer is enabled and not "busy". The paper cutter memory is programmed to initiate a cut cycle when the raster line over the writing head reaches the cutter blade. Cutting action is not guaranteed in 5000 series machines following a power failure. The command is immediate and does not interrupt.

1.2.4 Printer Enable:

This command assumes the printer is disabled and not "busy". The printer electronics are activated and the toning system is activated. The printer goes "busy" coincident with "enable" until the toning system is ready. An interrupt occurs following toning system "on", when "busy" status goes false.

1.2.5 Printer Disable/Alpha Select:

This command disables the printer. If "busy" was true when this command was issued, the operation in progress would compute before disabling occurred. The "alpha/graphic" mode control to the printer is set to "alpha".

1.2.6 Last Line Flag:

This command has two interpretations. If the printer is disabled prior to execution of this command and the "alpha/graphic" mode control is set to "graphic", this command conditions the printer/plotter to run in low-speed graphic mode.

If the printer is enabled prior to execution of this command and the "alpha/graphic" mode control is set to "graphic", this command conditions the printer/plotter to slow-down to a stop during output of the next two rasters of data. The command is immediate and does not interrupt.

1.2.7 Home Command:

This command requires the printer is enabled and not "busy". The paper is advanced 256 raster steps on roll or fan-fold equipped units. "Busy" status is reported until the operation completes. An interrupt is generated upon completion (when "busy" goes false).

1.2.8 Single Line Advance:

This command requires the printer is enabled and not "busy". The paper is advanced a single raster line or single character line according to the state of the alpha/graphic mode control. "Busy" is reported until the operation completes. An interrupts is generated when the command is accepted.

1.2.9 Other Commands:

Reset Command: This command will reset the device control logic, is issued through the BPIOC2 Control Register and is described in this appendix paragraph 2.4.2.

2.0 GOULD-SOC INSTRUCTION SET DESCRIPTION

2.1 OCP Instructions

2.1.1 OCP '0033, '0034

Start. This enables the BPIOC to transfer data, resets the data register, and resets the right-byte-next flag.

2.1.2 OCP '0133, '0134

Stop. This prevents further data transfer. The BPIOC must be stopped prior to a direction switch and prior to a control register change.

2.1.3 OCP '0233, '0234

Forward. This sets the forward/reverse flop. Issuing this command has the following results.

BPIOC1 - Enables data clocks to be sent to the device (GDATA).
BPIOC2 - Enables BPIOC2 Ready to be set automatically after having been reset due to an output function command (OTA).

2.1.4 OCP '0333, '0334

Reverse. This resets the forward/reverse flop. Issuing this command has the following results.

BPIOC1 - Disables data clocks to the device.
BPIOC2 - Disables the automatic setting of BPIOC2 Ready.

2.1.5 OCP '1433

DMA/C. This enables BPIOC1's DMA/C mode.

2.1.6 OCP '1533, '1534

Set Interrupt Mask.

2.1.7 OCP'1633, '1634

Reset Interrupt Mask.

2.1.8 OCP '1733, '1734

Initialize. This sets Stop and Forward. This resets the data register, right-byte-next, interrupt mask, DMA/C enable, and the control register (initial of input/output, non byte-pack, reset independent reverse and reset device enable.

2.2 SKS INSTRUCTIONS

2.2.1 SKS '0033, '0034

Skip if BPIOC is ready for data transfer.

2.2.2 SKS '0133

Skip if device is busy (moving paper, printing).

2.2.3 SKS '134

Skip if the device is selected (enabled).

2.2.4 SKS '0433, '0434

Skip if BPIOC not interrupting. The BPIOC will request an interrupt, if it is ready, in PIO (non DMA/C) mode and has its mask set.

2.3 INA INSTRUCTIONS

2.3.1 INA '34

Input device status if ready and input mode and "OR" with A. The INA resets ready.

2.3.2 INA '1034

Same as INA '0034 except that A is cleared prior to the operation. The status word returned is interpreted as follows:

Bit	1	2	3	4	5-15	16
1	Gould	Off-line	Vacuum Fault	Paper Low		Device Deselected
0		On-line				

Bit 1 always returns a "1" if a Gould Device is attached to the Controller.

Bit 2 defines the setting of the remote/local switch on the device.

Bit 3 (if a "1") indicates a vacuum fault has occurred during operation or device selection (enable function).

Bit 4 (if a "1") indicates that the paper supply is approaching depletion.

Bit 16 (if a "1") indicates that the device has deselected (timed out) in high speed plot mode and a gap (white area-s-) is intermingled with plot data.

2.3.3 INA '1133, '1134

Input ID. The ID of BPIOC(1) is ('101). The ID of BPIOC(2) is ('102).

2.3.4 INA '1433

Input DMA/C channel address.

2.3.5 INA '1633, '1634

Input interrupt vector.

2.4 OTA INSTRUCTIONS

2.4.1 OTA '0033, '0034

Output A to BPIOC data register if ready and output mode. The OTA resets BPIOC Ready.

2.4.2 OTA '1033, '1034

Output A to Control Register.

BPIOC1 control register bit description:

	Bit 13	Bit 14	Bit 15	Bit 16
1	Not used	Set to byte mode	———	———
0	Set to output mode	Set to word mode	———	———

BPIOC2 control register bit description:

	Bit 13	Bit 14	Bit 15	Bit 16
1	Set to input mode	Set to byte mode	Enable function strobe	Reset Gould
0	Set to output mode	Set to word mode	Disable function strobe	———

2.4.3 OTA '1433

Output DMA/C channel address. The format is as follows:

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5←→Bit 16
1	Input Transfer	———	1	DMC mode	Channel Address
0	Output Transfer	0	———	DMA mode	

2.4.4 OTA '1633,'1634

Output interrupt vector. The format is as follows:

	Bit 1←→Bit 4				Bit 5←→Bit 16
1	-	-	-	-	Interrupt Vector
0	0	0	0	0	

3.0 PROGRAMMING SEQUENCES

3.1 Device Status

Executing the following sequence will input the device status.

INA Device Status:

```
SB     BSS   1          Status Bin
STAT   DAC   **         Subr Entry Point
       OCP   '133       Disable BPIOC1 Operation
       OCP   '134       Disable BPIOC2 Operation
       OCP   '234       Set BPIOC2 to Forward Mode
                          (Enable Forward Data Strobe)
       LDA   ='14       Set BPIOC2 to Input Mode &
                          Byte Mode & Independent
       OTA   '1034        Forward Mode & Print Mode
       HLT   (or Error Exit)
       OCP   '34        Enable BPIOC2 Operation
       INA   '1034      Clear A and Read Device Status
                          Lines into A (via BPIOC2 data
                                                Register)
       HLT   (or Error Exit)
       STA   SB         Save Device Status
       JMP*  STAT       Exit
```

3.2 Function Commands

Each device requires a set of explicit function (control) commands for device control, paper motion and data printing. To properly issue these commands the following instructions sequences must be executed:

3.2.1 Paper Motion and Print Commands

Prior to issuing the "Home", "Feed", "Printer Enable", "Printer Disable", or "Print Line" command, the device "Busy" must be tested and verified false. When the device is issued a paper motion command, i.e., Feed or Home, it responds at the completion of paper motion to BPIOC2. This response will set BPIOC2 Ready. The setting of BPIOC2 Ready will cause an interrupt request if the BPIOC2 interrupt mask has been set. If the device is operated in an interrupt inhibited environment, completion can be tested with a skip if BPIOC2 is not interrupting or skip if BPIOC2 is ready instruction.

The paper motion and control sequence is as follows:

```
FB      BSS  1              Function Bin
FUNC    DAC  **             Subr Entry
        SKS  '133           Test for Device (Gould) Not Busy
        JMP  *-1            Wait or Error Exit

        OCP  '134           Disable BPIOC2 Operation
        OCP  '334           Set BPIOC2 to Reverse Mode
                              to Disable Automatic Set
                              of BPIOC2 Ready

        LDA  ='2            Set BPIOC2 to Output Mode &
        OTA  '1034            Word Mode & Independent Reverse
        HLT  (or Error Exit)  Mode & Not Reset
        OCP  '1534          Set BPIOC2 Interrupt Mask
                              (required if Interrupts
                              Enabled)
        OCP  '34            Enable BPIOC2 Operation
        LDA   FB            Load "A" with Function Code
        OTA  '34            Issue Command
        HLT  (or Error Exit)
Case 1: JMP*  FUNC          Exit if Interrupts Enabled
```

With Interrupts Disabled:

```
Case 2: SKS  '134           Test BPIOC2 Ready
        JMP   Case 2        Wait for Device Response to
                              Set BPIOC2 Ready
        JMP*  Func          Exit

Case 3: SKS  '434           Test BPIOC2 Interrupt Logic
        JMP*  Func          Exit when Device Response has
                              Set BPIOC2 Ready which in
                              this case, will result in an
                              Interrupt Request if the mask
                              is set.
        JMP   Case 3        Wait for Device Response
```

Both BPIOC1 and 2 are utilized to issue a print line command. This is due to the different manner in which the Gould device responds to this command. When the device is issued a Print Line command*, it responds at completion via its Data Request line. This response will set BPIOC1 Ready. The setting of BPIOC1 Ready will cause an interrupt request if BPIOC1 mask has been set. If the device is operated in an interrupt inhibited environment, completion can be tested with a skip if BPIOC1 is not interrupting or skip if BPIOC1 is ready instruction.

*via BPIOC2

The print line sequence is as follows:

```
PLC     DAC  **             Subr Entry
        SKS  '133           Test for Device (Gould) Not Busy
        JMP  *-1            Wait or Error Exit
        OCP  '133           Disable BPIOC1 Operation
        OCP  '134           Disable BPIOC2 Operation
        OCP  '333           Set BPIOC1 to Reverse Mode
                              (Inhibit Data Clock)
        OCP  '1533          Set BPIOC1 Interrupt Mask
                              (Required if Interrupts
                               Enabled)
        OCP  '33            Enable BPIOC1 Operation
        OTA  '33            Issue Psuedo Command to Reset
                              BPIOC1 Ready
        HLT  (or Error Exit)
        OCP  '34            Enable BPIOC2 Operation
        LDA ='11            Set A to Print Line Function
                              Code (see paragraph 1.0)
        OTA  '34            Issue Command
        HLT  (or Error Exit)

Case 1: JMP*  PLC           Exit if Interrupts Enabled
```

With Interrupts Disabled:

```
Case 2: SKS  '134           Test BPIOC1 Ready
        JMP   Case 2        Wait for Device Response to
                              Set BPIOC1 Ready
        JMP*  PLC           Exit

Case 3: SKS  '434           Test BPIOC1 Interrupt Logic
        JMP*  PLC           Exit when Device Response has
                              Set BPIOC1 Ready which in
                              this case will result in an
                              Interrupt Request if the
                              mask is set.
        JMP   Case 3        Wait for Device Response
```

3.3 High Speed Plot Mode

The Gould Device can plot data at two speeds. In the case of slow speed plot, the paper is slaved to the print line command, i.e., paper motion starts after data is plotted and stops after a scan line of motion. In the case of high speed plot, the paper feeds continuously and the data must be plotted within 2.5 milliseconds or the resulting plot will have blank (white) gaps imbedded in it. With continuous paper motion in effect the paper will move for 90 milliseconds after the device was issued a print command unless the appropriate action is taken. To overcome this constraint, the "last line" command must be issued two (2) lines in advance of the last plot line of data. In the event this operating criteria is not met, the device time out logic will be activated and the user must issue a "printer disable" or "reset" command in order to reset the time out condition and proceed with the device.

In order to correctly utilize this mode of operation, the following instruction sequence must be executed: (see paragraph 1.0)

1. Set the device to plot mode.

   a) Issue a "Printer Disable" (4_8) function command to the device.

   b) Issue a "Plot Mode Enable" (1_8) function command to the device.

   c) Issue a "Device Enable" (3_8) function command to the device.

   d) Output data to the device with provisions for sensing the next to last line of output, i.e., DMA End of Range at two lines before the output buffer is empty or at line count -2 if counting data output lines.

   e) Issue a "Last Line Flag Set" (5_8) function command to the device.

   f) Output the remaining two lines of data to the device.

3.4 Data Transfers

Data transfers take place via BPIOC1. These transfers can be implemented in programmed input-output (PI/O) mode or direct memory access (DMA/C) mode with interrupts enabled or disabled. In all cases, BPIOC1 must be set to output mode, with byte or word mode selected, independent reverse data strobe disabled, forward data strobe enabled and print or plot mode selected. The following sequences are examples of existing instructions used in test programs.

3.4.1 Gould Device (Not High Speed Plot) PI/O Mode Data Transfer (Interrupts Disabled)

Case 1: Output a block of data.

```
GPIO   DAC   **              Subr Entry
       OCP   '133            Disable BPIOC1 Operation
       OCP   '233            Enable Data Clock (Enable Forward
                               Data Strobe)
       OCP   '33             Enable BPIOC1 Operation
       LDA   ='4             Set BPIOC1 to Output Mode & Byte Mode
                               & Independent Forward Mode
                    } -or-
       LDA   ='1             Set BPIOC1 to Output Mode & Word
                               Mode & Independent Forward Mode
       OTA   '1033
       HLT   (or Error Exit)
```



```
       LDA   VPIOP           Set up Data Pointer and Word Count
       STA   OP
       LDA   VPIOC
       STA   OC
PIOD1  LDA*  OP              Get Data Word
       OTA   '33             Send it, if BPIOC1 is Ready
       JMP   *-1             BPIOC1 Not Ready.  Wait for Device
                               Ready to Set BPIOC1 Ready
       IRS   OP              Increment Pointer
       IRS   OC              Decrement Count
       JMP   PIOD1           Continue
       JMP*  GPIO            Exit
```

3.4.2 Gould Device (Not High Speed Plot) PI/O Mode Data Transfer (Interrupts Enabled)

Case 2: Output a word of data.

```
GPIO   DAC   **              Subr Entry
       OCP   '133            Disable BPIOC1 Operation
       OCP   '233            Enable Data Clock (Enable Forward
                               Data Strobe
       OCP   '1533           Set BPIOC1 Interrupt Mask
       OCP   '33             Enable BPIOC1 Operation
       LDA   ='4             Set BPIOC1 to Output Mode & Byte Mode
                               & Independent Forward Mode
                    } -or-
       LDA   ='0             Set BPIOC1 to Output Mode & Word
                               Mode & Independent Forward Mode
       OTA   '1033
       HLT   (or Error Exit)
       LDA    Data Word      Get Data Word
       OTA   '33             Send it
       HLT   (or Error Exit)
       ENB                   Enable Interrupts
       JMP*  GPIO            Exit and Wait for Device Ready to Set
                               BPIOC1 Ready which will result in
                               a BPIOC1 interrupt request.
```

Gould Device (Not High Speed Plot)

3.4.3 DMA Mode Data Transfer (With Interrupts Enabled)

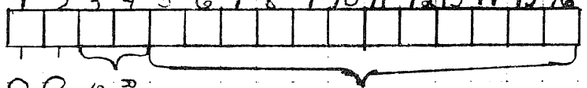
```
GDMA    DAC   **              Subr Entry
        OCP   '133            Disable BPIOC1 Operation
        OCP   '233            Enable Data Clock (Enable Forward
                                Data Strobe)
        OCP   '1433           Set BPIOC1 to DMA/C Mode
        OCP   '1533           Set BPIOC1 Interrupt Mask
        LDA   ='4             Set BPIOC1 to Output Mode & Byte Mode
                                & Independent Forward Mode
                    -or-
        LDA   ='1             Set BPIOC1 to Output Mode & Word Mode
                                & Independent Forward Mode
        OTA   '1033
        HLT   (or Error Exit)
        LDA   ='200XX         Set BPIOC1 to DMA & Output Mode where
                                XX is the Even Address of an Even
                                Odd Channel Pair in Register File
                                (Addresses 20₈ to 37₈)
        OTA   '1433
        HLT   (or Error Exit)
        LDA   =VINTHP         Set up Interrupt Vector Address
        OTA   '1633
        HLT   (or Error Exit)
        LDA   VDMAC           Set DMA Word Count, using Channel
                                Pair 20 and 21
        STA   '20
        LDA   VDMAP           Set Beginning Address
        STA   '21
        OCP   '33             Start DMA Transfers
        ENB                   Enable Interrupts
        JMP*  DMAD            Exit and wait for DMA End of Range to
                                set BPIOC1 Interrupt Reguest
```


Gould Device (Not High Speed Plot)

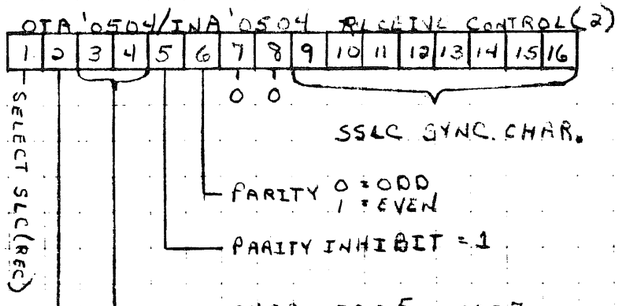
3.4.4 DMC Mode Data Transfer (with Interrupts Enabled)

```
GDMC    DAC   **              Subr Entry
        OCP   '33             Disable BPIOC1 Operation
        OCP   '233            Enable Data Clock (Enable Forward
                                Data Strobe)
        OCP   '1433           Set BPIOC1 to DMA/C Mode
        OCP   '1533           Set BPIOC1 Interrupt Mask
        LDA   ='4             Set BPIOC1 to Output Mode & Byte
                                Mode & Independent Forward Mode
                    -or-
        LDA   ='1             Set BPIOC1 to Output Mode & Word
                                Mode & Independent Forward Mode
        OTA   '1033
        HLT   (or Error Exit)
        LDA   ='3XXXX         Set BPIOC1 to DMC Mode where XXXX is
                                the Even Address of an Even Odd
                                Channel Pair, in memory, which
                                contains the beginning address of
                                the data to be transferred followed
                                by the ending address of the data
                                to be transferred in the odd address.
        OTA   '1433
        HLT   (or Error Exit)
        OCP   '33             Enable BPIOC1 Operation
        ENB                   Enable Interrupts
        JMP*  GDMC            Exit and wait for DMC End of Range
                                to set BPIOC1 Interrupt Request
```

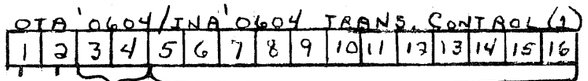
OTA'0404/INA'0404 RECEIVE CONTROL (1)



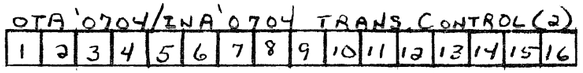
OTA'0504/INA'0504 RECEIVE CONTROL (2)



OTA'0604/INA'0604 TRANS. CONTROL (1)



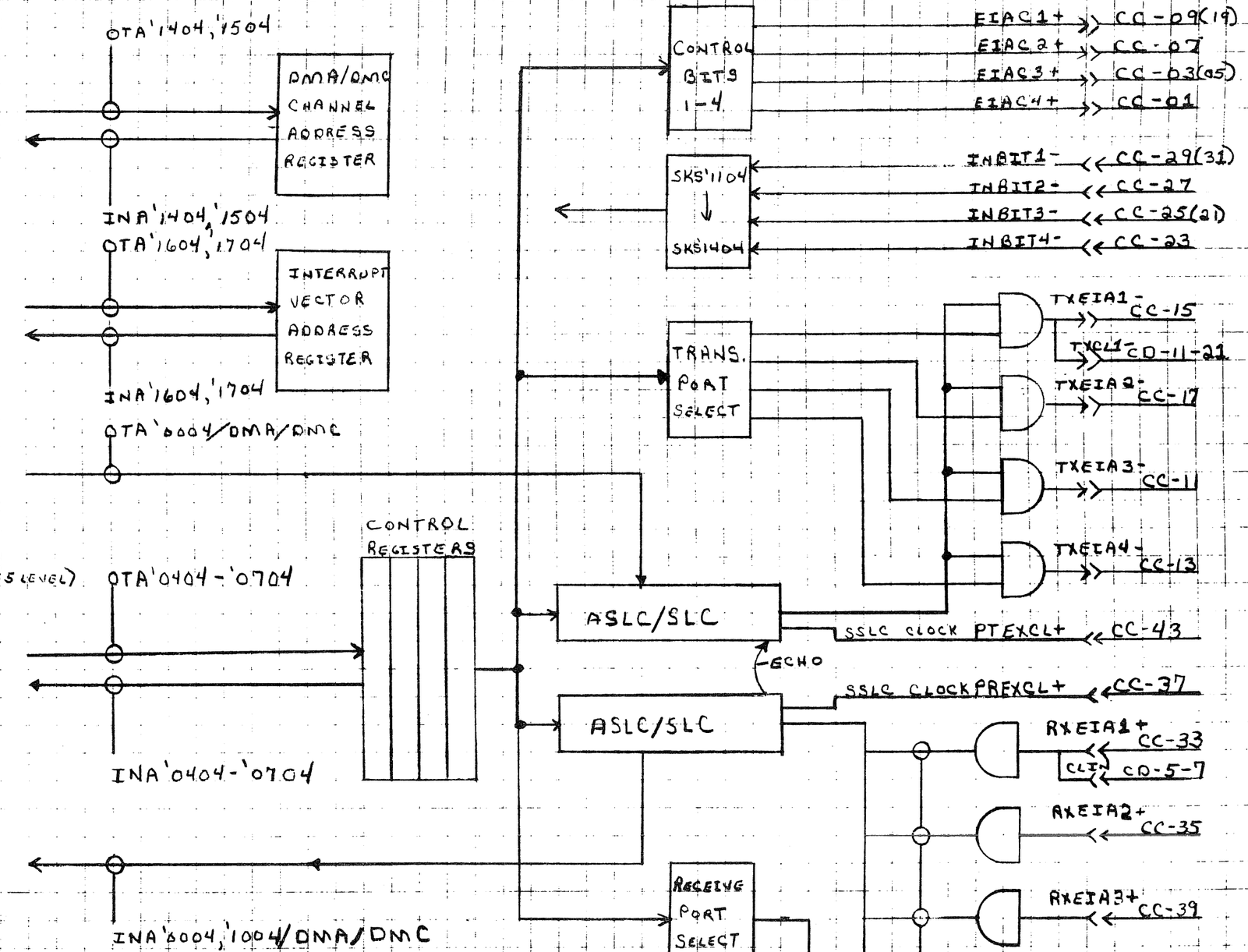
OTA'0704/INA'0704 TRANS. CONTROL (2)



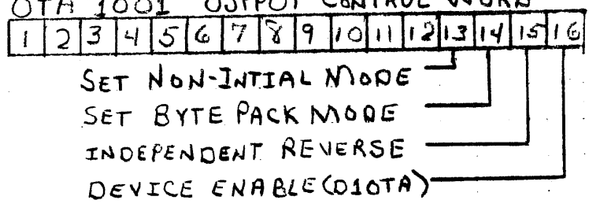
THE BIT BREAKDOWN IS THE SAME AS OTA'0504, EXCEPT IT IS FOR THE TRANSMIT

NOTE 1

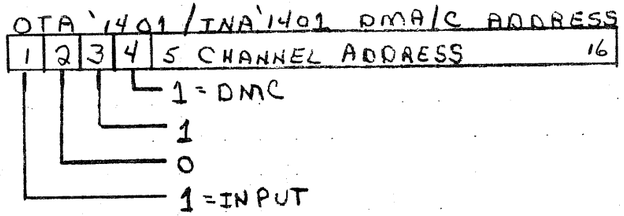
N=	BAUD=	N=	BAUD=
'17	75	'373	1800
'27	110	'767	2400
'37	150	'1756	4800
'76	300	'3735	9600
'175	600		



OTA '1001 OUTPUT CONTROL WORD

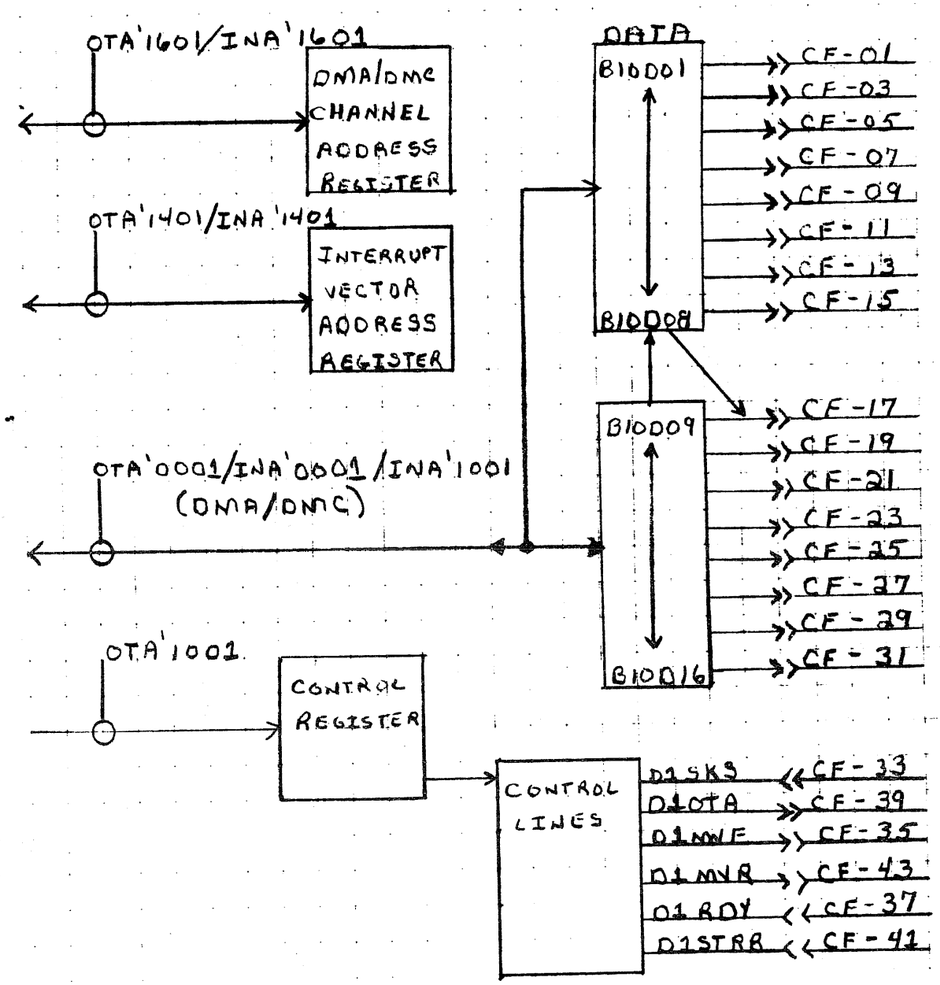


OTA '1401 / INA '1401 DMA/C ADDRESS



NOTES

1. THE BPIOC, IN BYTE PACK MODE, HANDLES THE MOST SIGNIFICANT BYTE FIRST
2. THE SOC HAS OPTIONAL TWO BPIOC's. DEVICE ADDRESS 01 AND 02
3. CONTROL REGISTER BIT 15 SETS REVERSE OCP '0301 INHIBITS FORWARD



NAME	SOURCE	DESCRIPTION
D1SKS	DEVICE	SKŜ0101
D1OTA	CONTROLLER	OTA '1001 BIT 16
D1MWF	CONTROLLER	FORWARD STROBE
D1MVR	CONTROLLER	REVERSE STROBE
D1RDY	DEVICE	DEVICE READY
D1STRB	DEVICE	DEVICE STROBE

LTR	DATE	REVISION	DR.	CK.

SHEETS

OPTION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	WIRE LIST
SOC	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	✓	X	X	X	X	X	X	X						X	X		X	X	X	X		
VERSATEC	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	27A	28A	29A	30A	31A	32A	33A															
GOULD	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	27B	28A	29B	30B	31B	32B	33B	X														

III-01

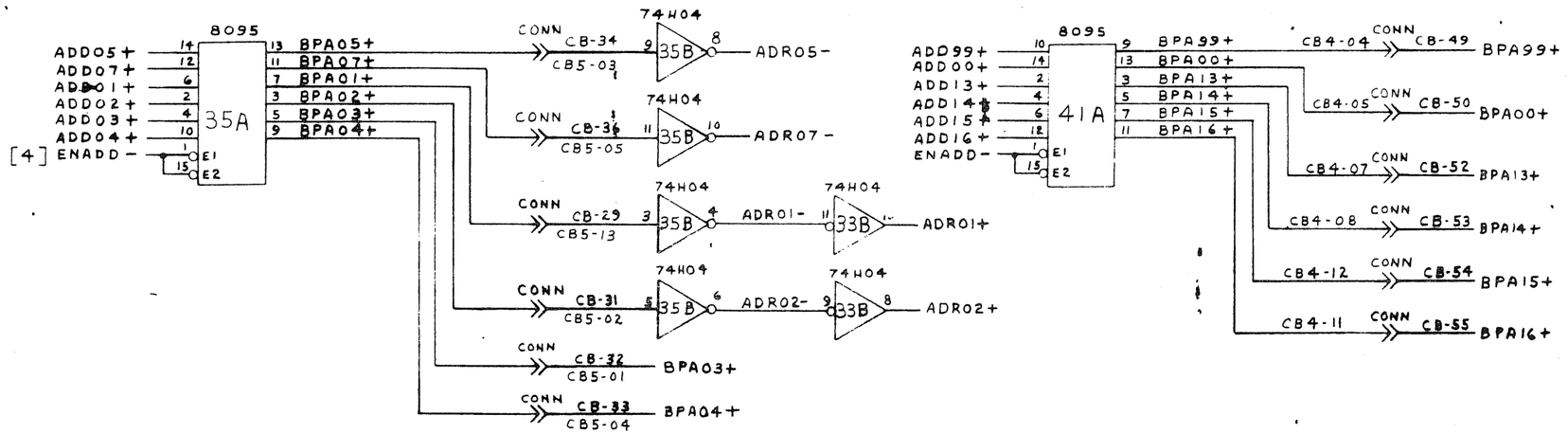
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	DIRECTORY SOC	
	APPRD		
	USED ON NEXT ASSY	SCALE SHEET OF	SIZE C DWG. NO. LBD1528 REV

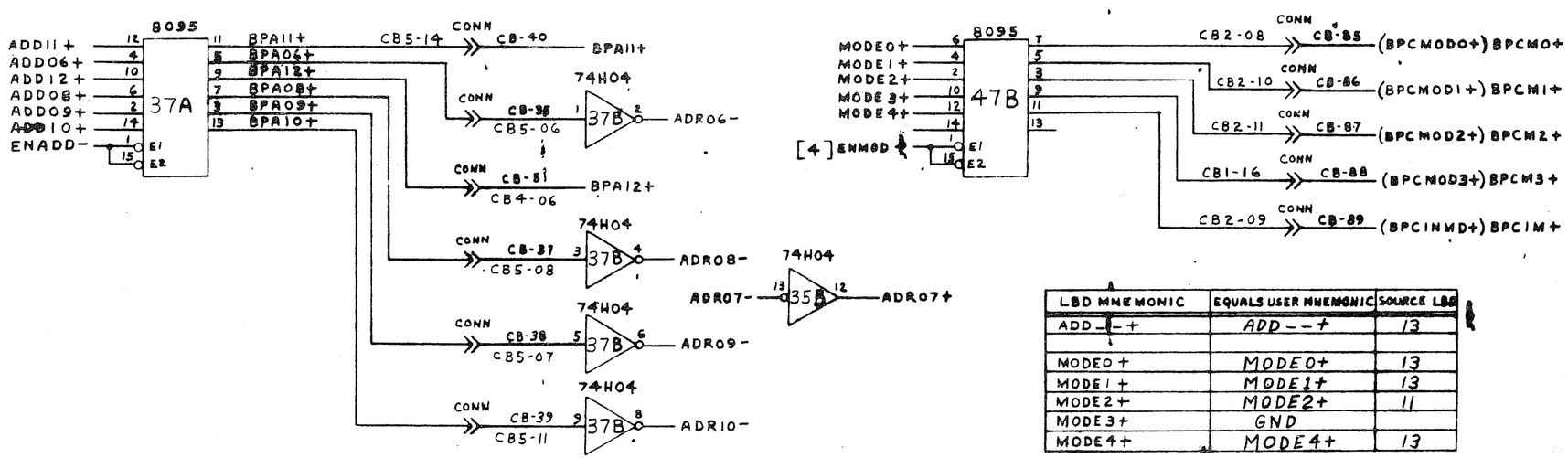
LTR	DATE	REVISION	DR.	CR.
		ENGINEERING CHANGE NOTICE	DATE	
			5-1-74	200.
			5-7-74	
			5-31-74	
			6-27-74	
		RELEASED AT WL REV 3	7-10-74	RK M.S.
		WL REV 4 PER ECN 1457 W.L. REV. 5 PER ECN 1461	10-8-74	RK M.S.
		ADDED SHT 44 THRU 47 MODEL # 3000, 30-1, 3025	10-11-74	RK MS
		WL REV 6 PER ECN 1523 W.L. REV. 7 PER ECN 1544	1-9-75	RK MS
		WL REV 7 PER ECN 1548	3-18-75	RK MS
		WL REV 9 PER ECN 1586	5-14-75	RK MS
		ADDED SHEETS	8-1-75	PB
		W.L. REV. 10 ECN 1626	8-5-75	PB MS
		RELEASED	8-27-75	PB RLW
		PER ECR 1642 & 1644	11-21-75	LTS.
		PER ECR 1725	2-2-76	LTS.
		PER ECR 1727	3-17-76	LTS

REVISION LEVEL

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .03 .XXX ± .005 ANGLES ± 1/2°	CHK 7/9/74 ENG. APPRD	REVISION STATUS SHEET WW
	USED ON NEXT ASSY MEC8027	SCALE SHEET 1 OF 11 SIZE C DWG. NO. LBD1528 REV K

III-02



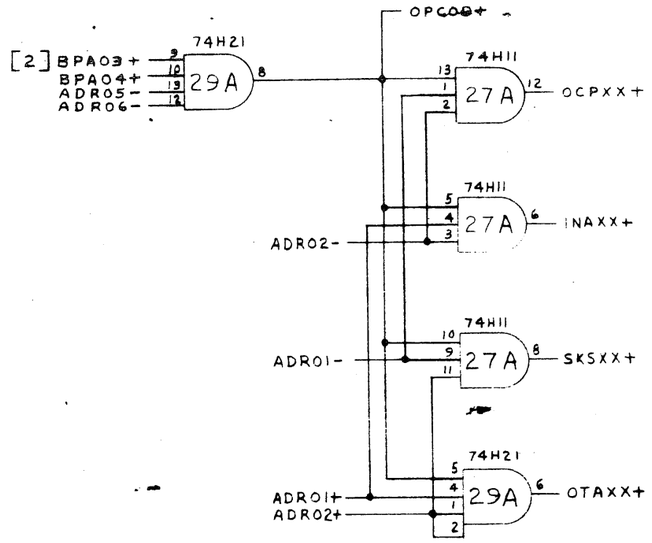


I/O BUS ADDRESS
DRIVERS & RECEIVERS

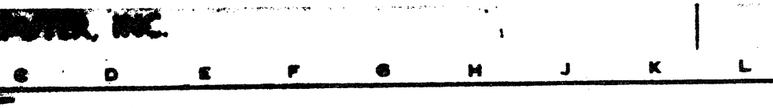
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD--+	ADD--+	13
MODE0+	MODE0+	13
MODE1+	MODE1+	13
MODE2+	MODE2+	11
MODE3+	GND	
MODE4+	MODE4+	13

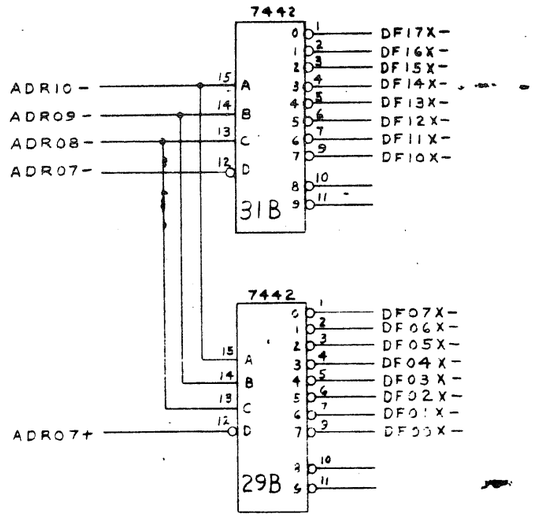
III-03

MATERIAL
DWN J. Bojan 3/14/74
CHK
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I/O BUS INTERFACE LOGIC
ADDRESS AND MODE LINES
SOC WW
SIZE C LBD 128

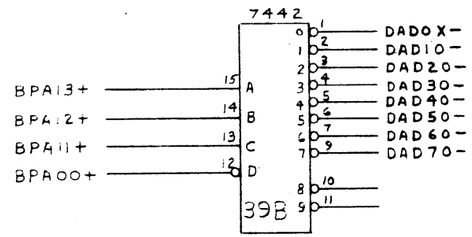


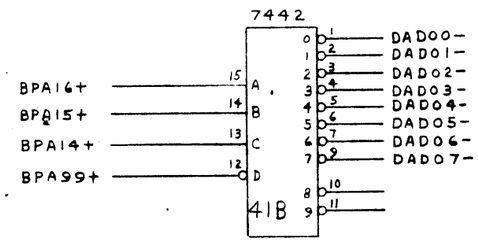
CP CODE DECODE





FUNCTION DECODERS



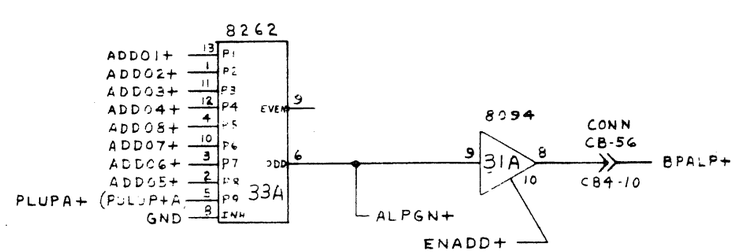


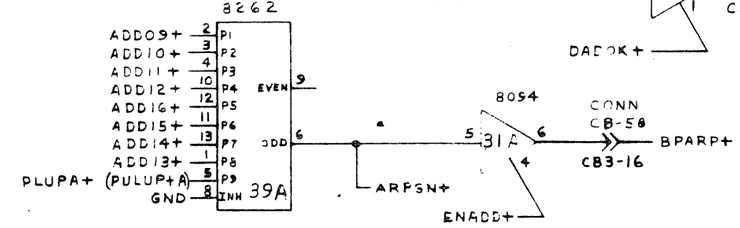
OCTAL ADDRESS DECODERS

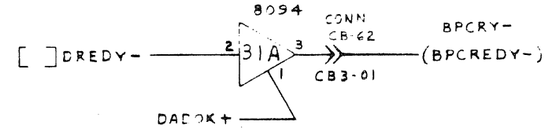
II-04

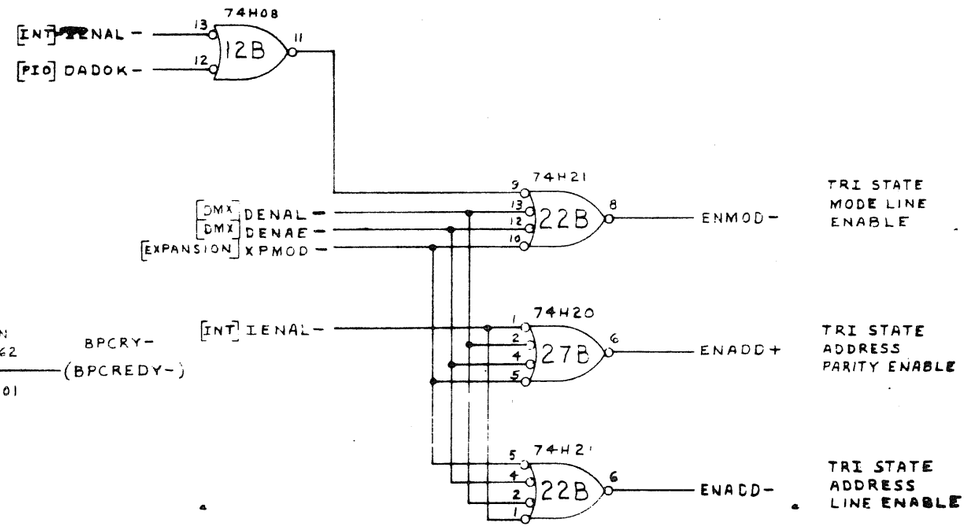
MATERIAL	DRWN W Bogan 3/14/74	PRIME COMPUTER, INC. MATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC ADDRESS DECODING SOC WW III
	ENGR	
	APPRD	
		SIZE C DWG. NO. LBD1528 REV. A

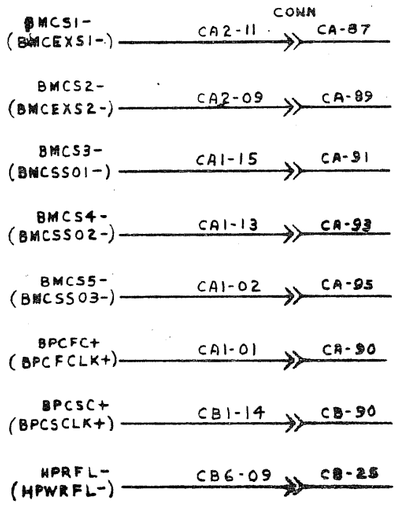
PRP-003



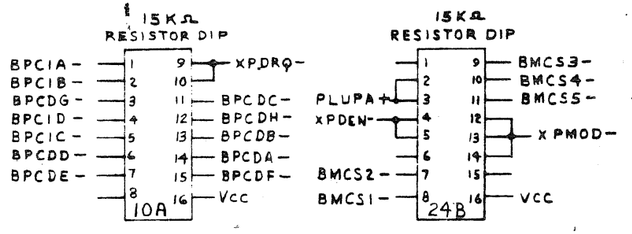








LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD__+	ADD__+	13
DADOK-	DADOK-	10
XPMOD-		
XPDEN-		
INAOK-	INAOK-	10
XPDEE-		
DREDY-	DREDY-	10
DADOK+	DADOK+	10



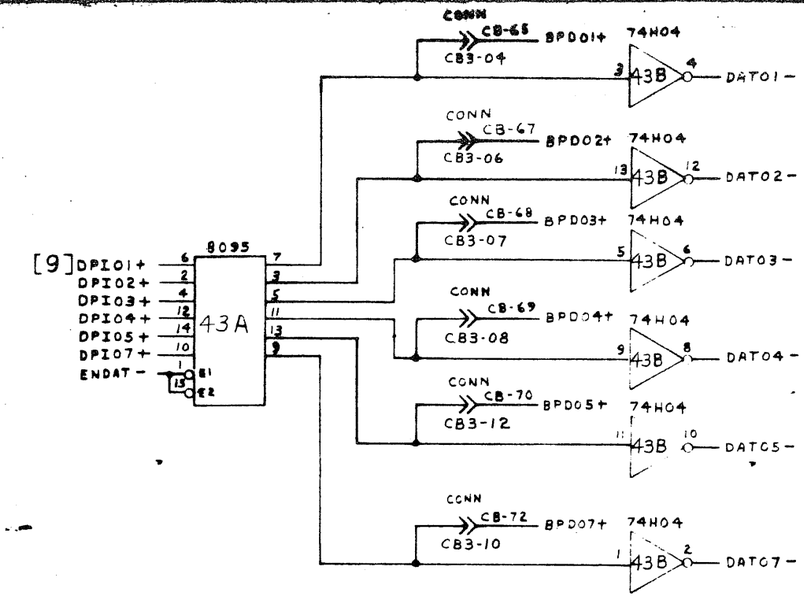
MATERIAL

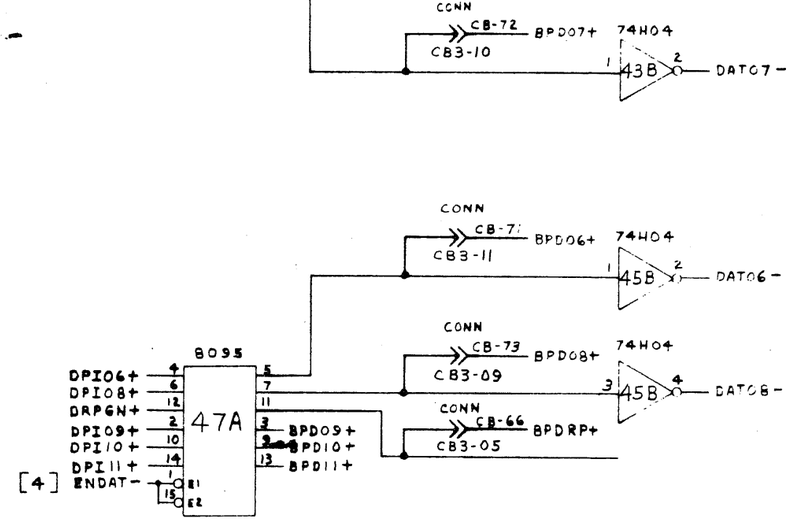
DRN W. Bogan 3/4/74

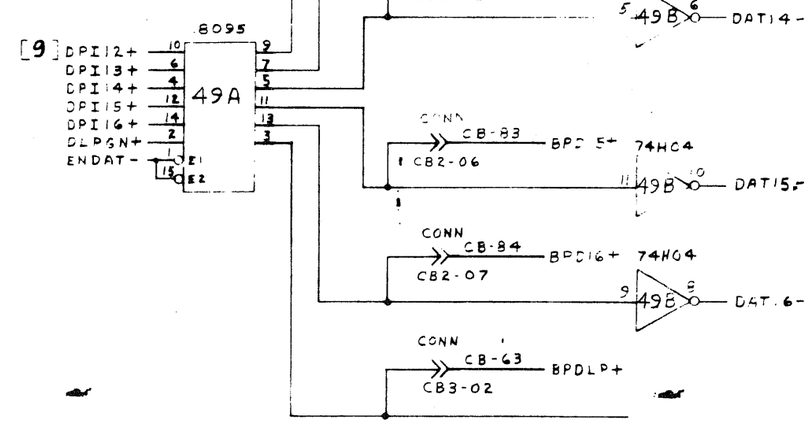
CHK

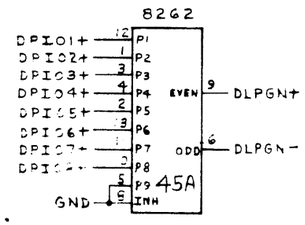
PRIME COMPUTER, INC.

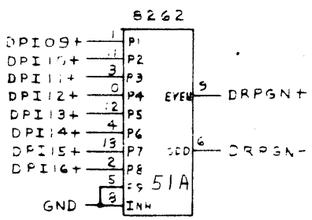
I/O BUS INTERFACE LOGIC
ADDRESS FAMILY







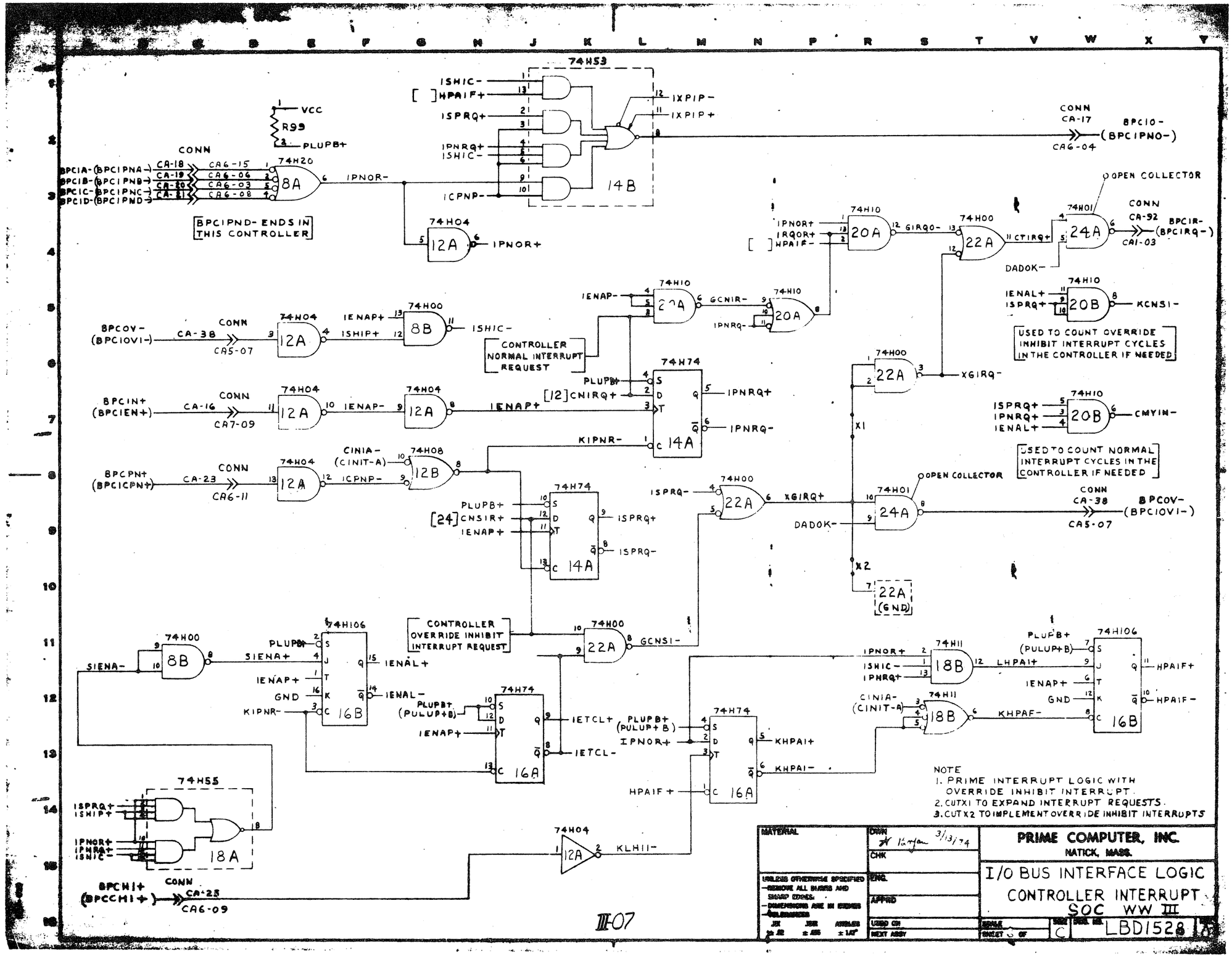


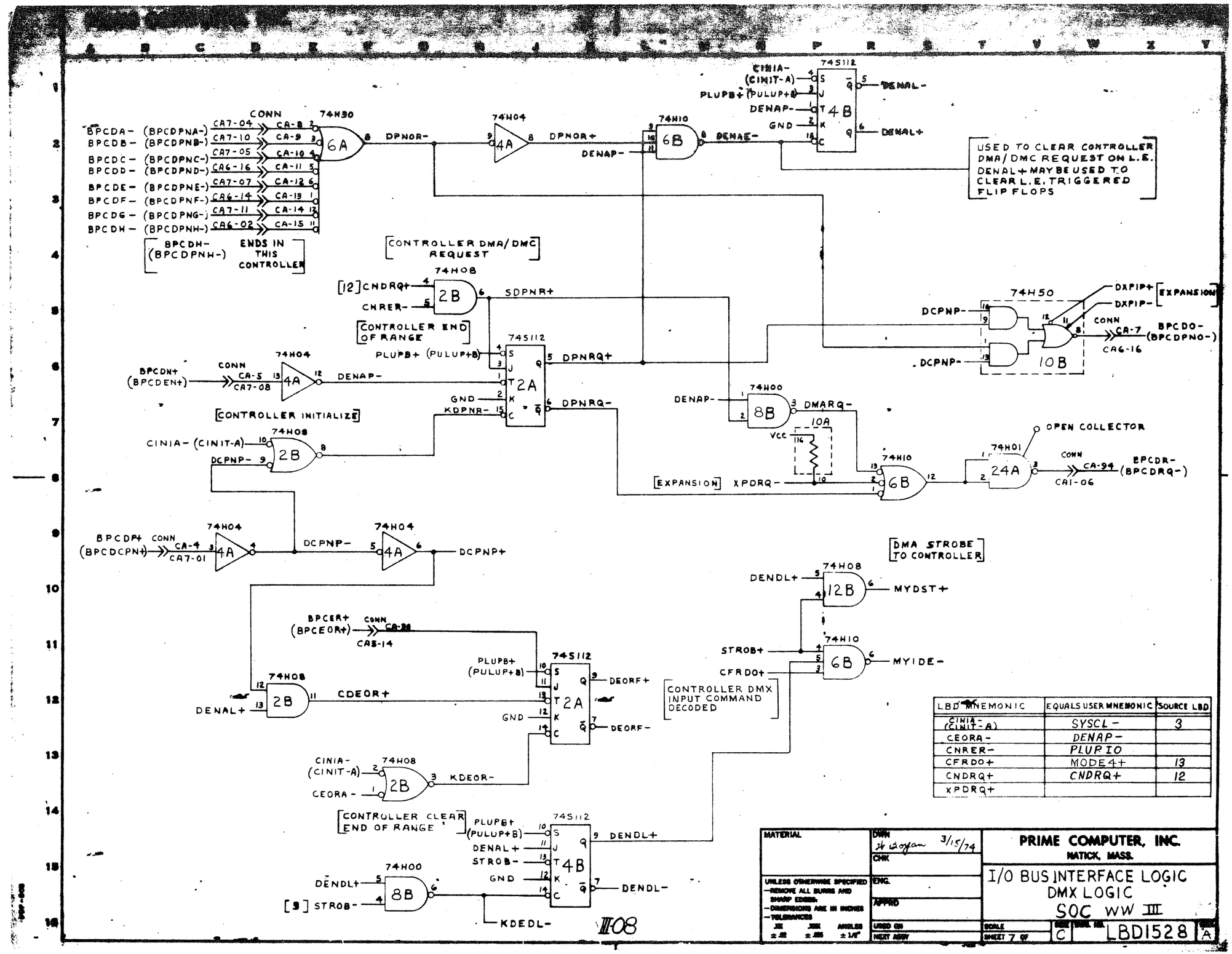


LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
DPIXX+	DPIXX+	9

III-06

MATERIAL	DWN 3/5/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	I/O BUS INTERFACE LOGIC
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	DATA BUS LINES SOC WW III
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 5 OF
		SIZE C DWG. NO. LBD1528 REV. A

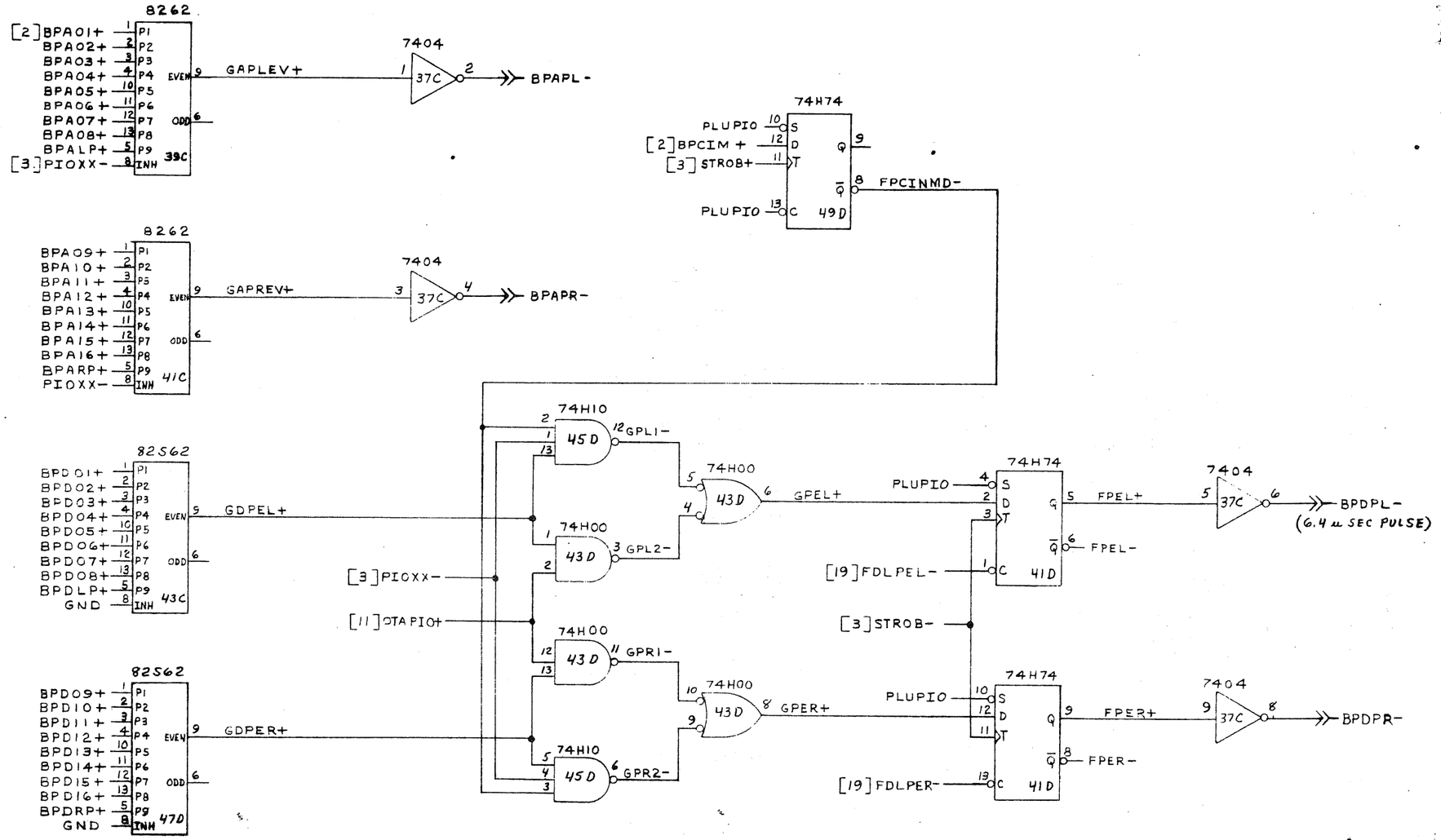

74H53
ISHIC-
HPAIF+
ISPRQ+
IPNRQ+
ISHIC-
ICPNP-
IXPIP-
IXPIP+
14B
VCC
R99
PLUPB+
CONN
BPCIA-(BPCIPNA-) CA-18 CA6-15
BPCIB-(BPCIPNB-) CA-19 CA6-06
BPCIC-(BPCIPNC-) CA-20 CA6-03
BPCID-(BPCIPND-) CA-21 CA6-08
74H20
8A
IPNOR-
BPCIPND- ENDS IN THIS CONTROLLER
74H04
12A
IPNOR+
CONN
CA-17
CA6-04
BPCIO-
(BPCIPNO-)
OPEN COLLECTOR
74H10
20A
IPNOR+
IRQOR+
HPAIF-
GIRQO-
74H00
22A
CTIRQ+
74H01
24A
CONN
CA-92
CA1-03
BPCIR-
(BPCIRQ-)
DADOK-
IENAP-
74H10
20A
GCNIR-
IPNRQ-
20A
74H10
IENAL+
ISPRQ+
20B
KCNS1-
USED TO COUNT OVERRIDE INHIBIT INTERRUPT CYCLES IN THE CONTROLLER IF NEEDED
BPCOV-
(BPCIOVI-)
CONN
CA-38
CA5-07
74H04
12A
IENAP+
ISHIP+
74H00
8B
ISHIC-
CONTROLLER NORMAL INTERRUPT REQUEST
74H74
PLUPB+
[12]CNIRQ+
IPNRQ+
IPNRQ-
14A
74H00
22A
XGIRQ-
X1
BPCIN+
(BPCIEN+)
CONN
CA-16
CA7-09
74H04
12A
IENAP-
12A
IENAP+
KIPNR-
74H10
20B
CMYIN-
ISPRQ+
IPNRQ+
IENAL+
USED TO COUNT NORMAL INTERRUPT CYCLES IN THE CONTROLLER IF NEEDED
BPCPN+
(BPCICPN+)
CONN
CA-23
CA6-11
74H04
12A
ICPNP-
CINIA-
(CINIT-A)
74H08
12B
74H74
PLUPB+
[24]CNSIR+
IENAP+
ISPRQ+
ISPRQ-
14A
74H00
22A
XGIRQ+
ISPRQ-
DADOK-
74H01
24A
OPEN COLLECTOR
CONN
CA-38
CA5-07
BPCOV-
(BPCIOVI-)
X2
22A
(GND)
CONTROLLER OVERRIDE INHIBIT INTERRUPT REQUEST
74H00
22A
GCNSI-
74H106
16B
PLUPB+
SIENA+
IENAP+
GND
KIPNR-
IENAL+
IENAL-
SIENA-
74H00
8B
74H74
PLUPB+ (PULUP+B)
IENAP+
IETCL+
IETCL-
16A
74H74
PLUPB+ (PULUP+B)
IPNOR+
KHPAI+
KHPAI-
HPAIF+
16A
74H11
18B
IPNOR+
ISHIC-
IPHRQ+
LHPAI+
74H106
16B
PLUPB+ (PULUP+B)
IENAP+
GND
HPAIF+
HPAIF-
74H11
18B
CINIA- (CINIT-A)
KHPAF-
74H55
ISPRQ+
ISHIP+
IPNOR+
IPNRQ+
ISHIC-
18A
74H04
12A
KLHII-
BPCHI+
(BPCCHI+)
CONN
CA-25
CA6-09
NOTE
1. PRIME INTERRUPT LOGIC WITH OVERRIDE INHIBIT INTERRUPT.
2. CUTX1 TO EXPAND INTERRUPT REQUESTS.
3. CUT X2 TO IMPLEMENT OVERRIDE INHIBIT INTERRUPTS
III-07
MATERIAL
UNLESS OTHERWISE SPECIFIED
-REMOVE ALL BURRS AND SHARP EDGES.
-DIMENSIONS ARE IN INCHES
-TOLERANCES
.XX .XXX ANGLES
± .02 ± .005 ± 1/2°
DRWN 3/13/74
CHK
ENG.
APPRD
USED ON
NEXT ASSY
PRIME COMPUTER, INC.
NATICK, MASS.
I/O BUS INTERFACE LOGIC
CONTROLLER INTERRUPT
SOC WW III
SIZE C
DWG. NO. LBD1528
SCALE
SHEET 5 OF



LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIA- (CINIT-A)	SYSCL-	3
CEORA-	DENAP-	
CNRER-	PLUP IO	
CFRDO+	MODE4+	13
CNDRQ+	CNDRQ+	12
XPDRQ+		

MATERIAL	DWN H Logan 3/15/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	I/O BUS INTERFACE LOGIC DMX LOGIC SOC WW III
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 7 OF
		SIZE C — DRAWING NO. LBD1528 — REV A

III-08



MATERIAL	DWN H. Bryan 1/22/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ± 1/2°	ENG.	SOC I/O BUS {ADDRESS} PARITY CHECK {DATA}
	APPRD	
	USED ON	
	NEXT ASSY	SCALE SHEET 8 OF 16 · SIZE C · DWG. NO. LBD1528 · REV E

II-09

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74153 45C: PLUPIO, B12D01+, MODE4+ [13] [25], CLKD01+, PLUPIO, B12D02+, FDAT2+, CLKD02+, DATS1B+, DATS1A+, ENBD18− → DPI01+, DPI02+

74153 47C: PLUPIO, B12D03+, MODE1+, CLKD03+, BMCS1−, B12D04+, MODE0+, CLKD04+ → DPI03+, DPI04+

74153 49C: BMCS2−, B12D05+, ADD05+, CLKD05+, BMCS3−, B12D06+, ADD06+, CLKD06+ → DPI05+, DPI06+

74153 51C: BMCS4−, B12D07+, ADD07+, CLKD07+, BMCS5−, B12D08+, ADD08+, CLKD08+ → DPI07+, DPI08+

74157 27H: BPID01+, BP2D01+, BPID02+, BP2D02+, BPID03+, BP2D03+, BPID04+, BP2D04+, DATS82+, GND → B12D01+, B12D02+, B12D03+, B12D04+

74157 29H: BPID05+, BP2D05+, BPID06+, BP2D06+, BPID07+, BP2D07+, BPID08+, BP2D08+, GND → B12D05+, B12D06+, B12D07+, B12D08+

74157 27G: BPID09+, BP2D09+, BPID10+, BP2D10+, BPID11+, BP2D11+, BPID12+, BP2D12+, GND → B12D09+, B12D10+, B12D11+, B12D12+

74157 29G: BPID13+, BP2D13+, BPID14+, BP2D14+, BPID15+, BP2D15+, BPID16+, BP2D16+, GND → B12D13+, B12D14+, B12D15+, B12D16+

74153 45E: RXS09+, B12D09+, ADD09+, CLKD09+, RXS10+, B12D10+, ADD10+, CLKD10+, DATS1B+, DATS1A+, GND → DPI09+, DPI10+

74153 47E: RXS11+, B12D11+, ADD11+, CLKD11+, RXS12+, B12D12+, ADD12+, CLKD12+ → DPI11+, DPI12+

74153 49E: RXS13+, B12D13+, ADD13+, CLKD13+, RXS14+, B12D14+, ADD14+, CLKD14+ → DPI13+, DPI14+

74153 51E: RXS15+, B12D15+, ADD15+, CLKD15+, RXS16+, B12D16+, ADD16+, CLKD16+ → DPI15+, DPI16+

74H50 33G: SOCDMX+, FDXSB−, GADRT+, DF00/10+ → ENBD18+

74H04 20D: ENBD18+ → GNBD18−

74157 49F: GND, [16] RXD03+, PLUPIO, RXD10+, GND, RXD11+, [10] DADCLK+, RXD12+, GND; GADRT−, SOCDMX− → DATSRT+; RXS09+, RXS10+, RXS11+, RXS12+

74157 51F: GND, RXD13+, DADRT+, RXD14+, DADBP2+, RXD15+, DADBP1+, RXD16+, DATSRT+, GND → RXS13+, RXS14+, RXS15+, RXS16+

74H00 31F: GADRT−, SOCDMX− → DATSRT+

74H00 33E: GADCLK−, GRE− → DATSIB+

74H00 31F: SOCDMX+, FDXSB+ → GDXSB−

74H20 33D: GDXSB−, GADCLK−, GADBP1−, GADBP2− → DATSIA+

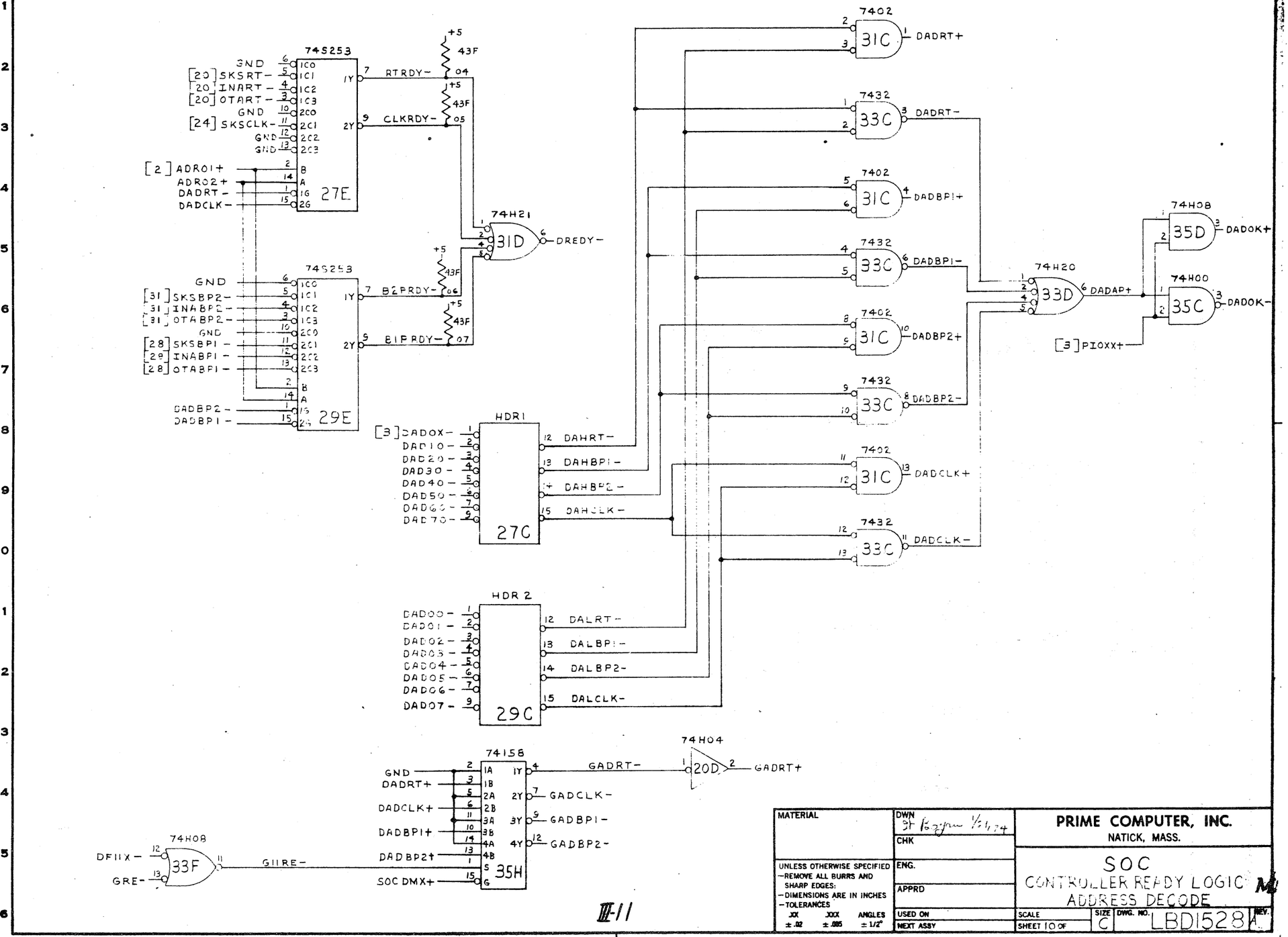
74H00 31F: SOCDMX+, FDXSA+ → GDXSA−

74H00 27F: GDXSA−, GADBP2− → DATSB2+

III-10

PDF-003

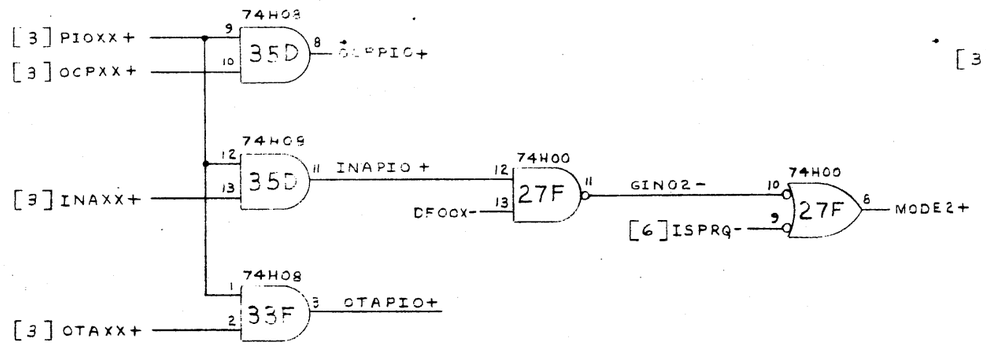
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC DATA MUX	
	APPRD		
USED ON / NEXT ASSY	SCALE / SHEET OF	SIZE C / DWG. NO. LBD1528	REV. A

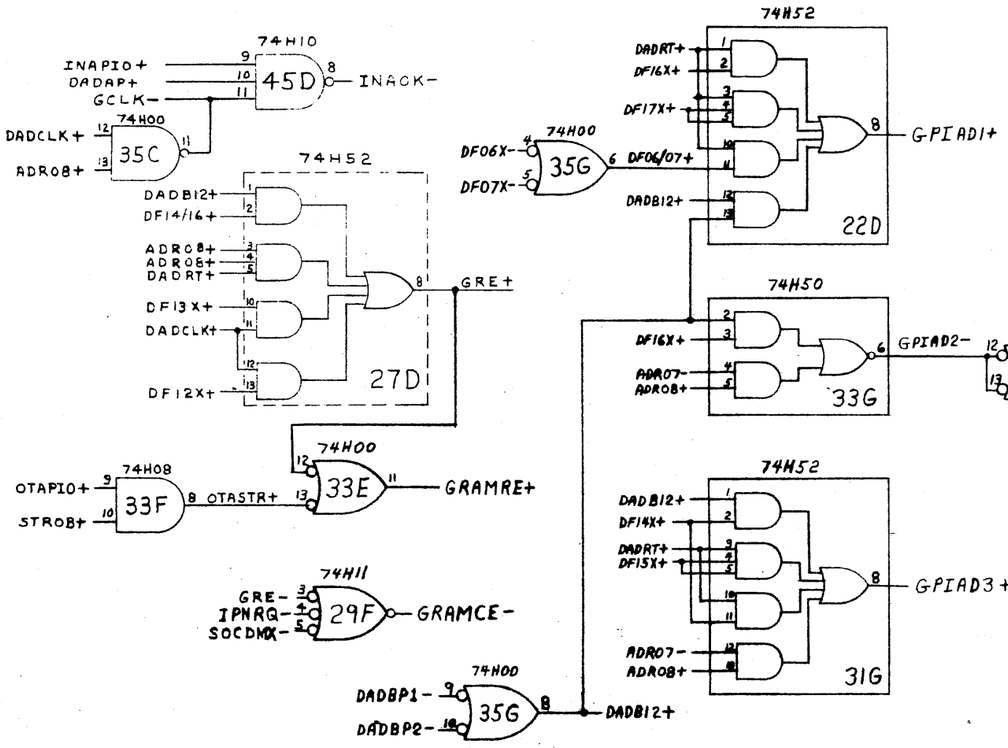


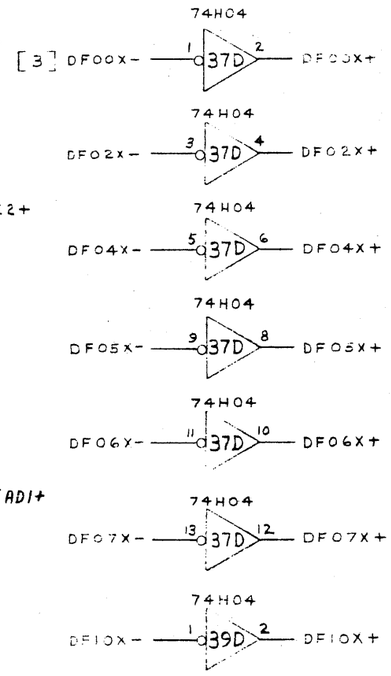
III-11

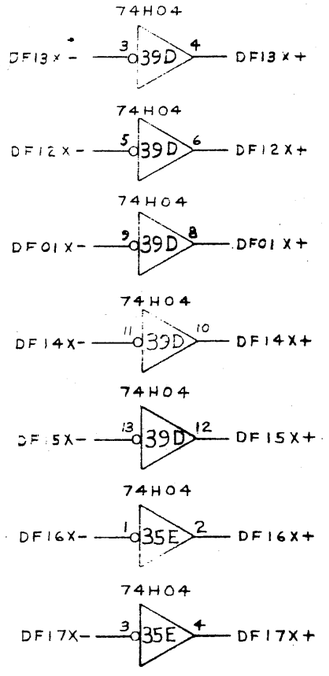
MATERIAL	DWN ST 12-7-74 1:1	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	SOC CONTROLLER READY LOGIC ADDRESS DECODE	
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 10 OF	SIZE C / DWG. NO. LBD1528 / REV. A

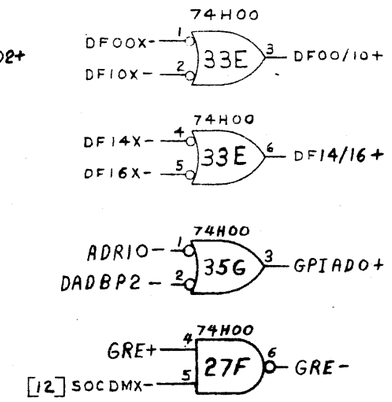
PDF-003

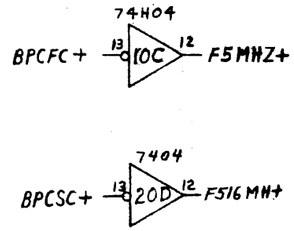




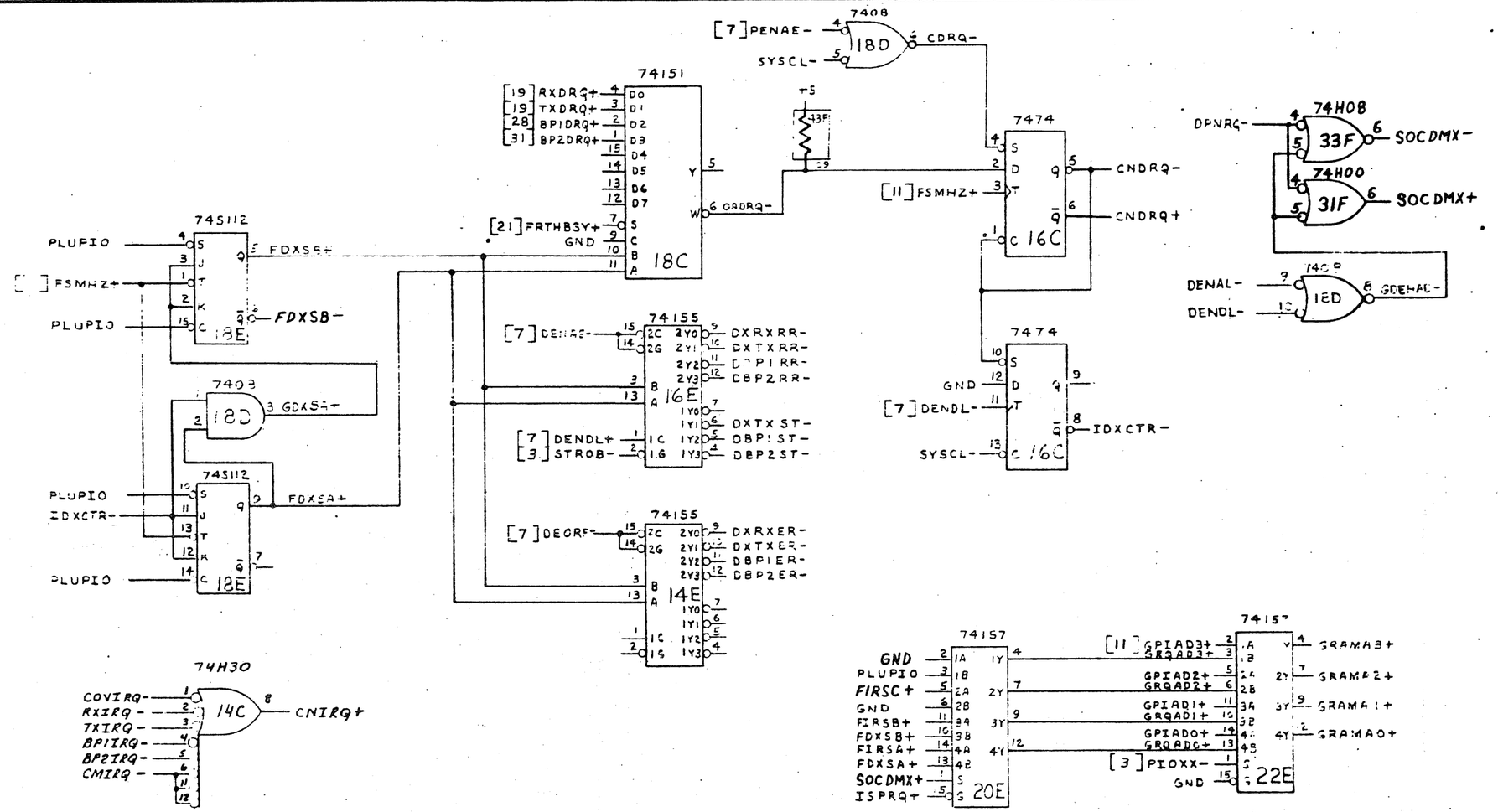








MATERIAL	DWN M. Bogan 3/28/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC MISC I/O BUS RECEIVERS
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 17
		SIZE C LBD1528



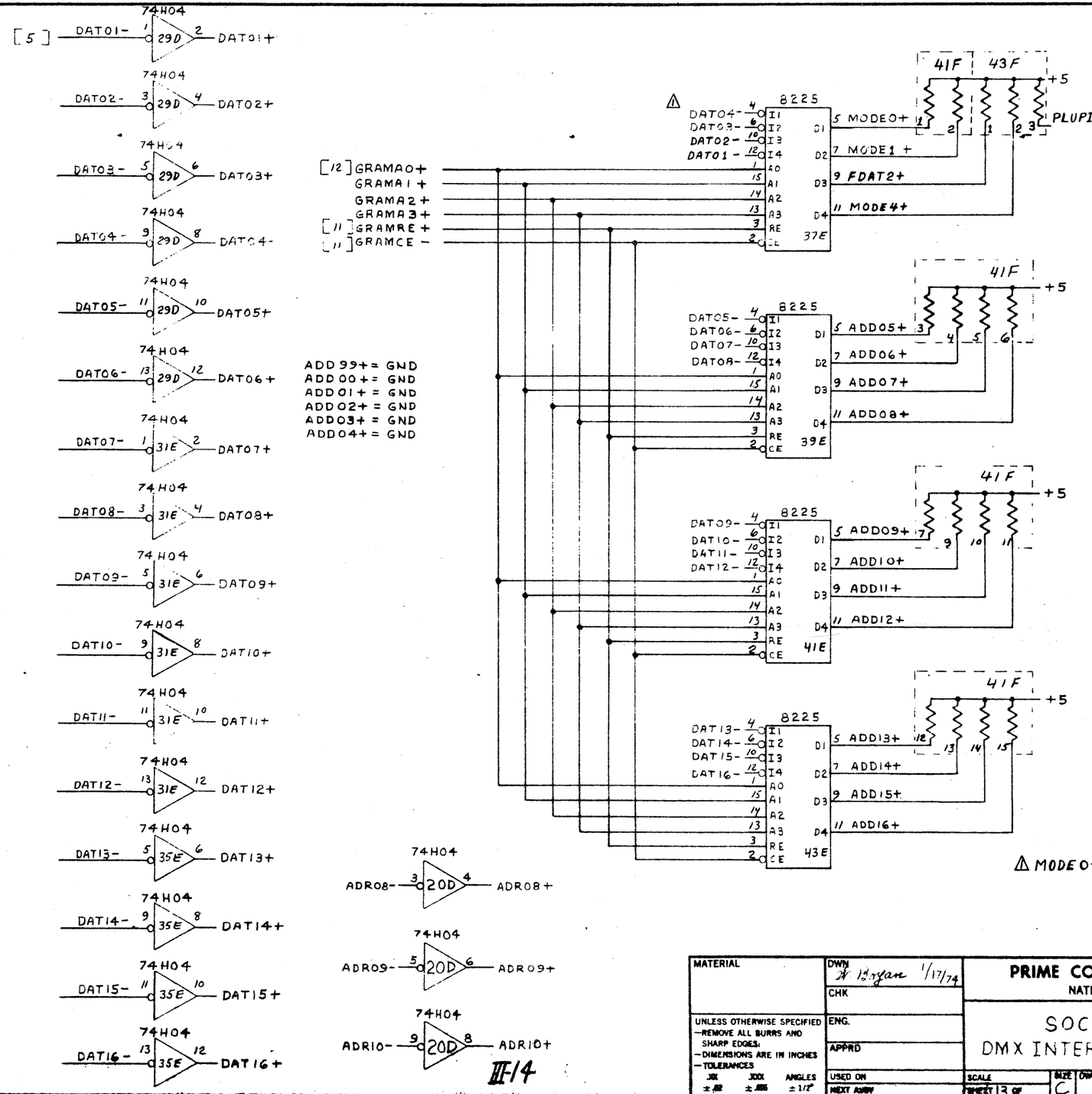
DEFINED RAM LOCATIONS

DMA	INTERRUPT		PIO	
RX'10	CLOCK MI	0	RXC1	'14
TX'11	CLOCK OV	1	RXC2	'15
BP1'12	RX	2	TXC1	'16
BP2'13	TX	3	TXC2	'17
	BP1	6		
	BP2	7		

MATERIAL	DWN JL Gorman 4/3/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC DMX INTERRUPT INTERNAL CONTROL	
	APPRD		
	USED ON	SCALE	SIZE C — DWG. NO. LED1528 — REV. B
	NEXT ASSY	SHEET 13 OF	

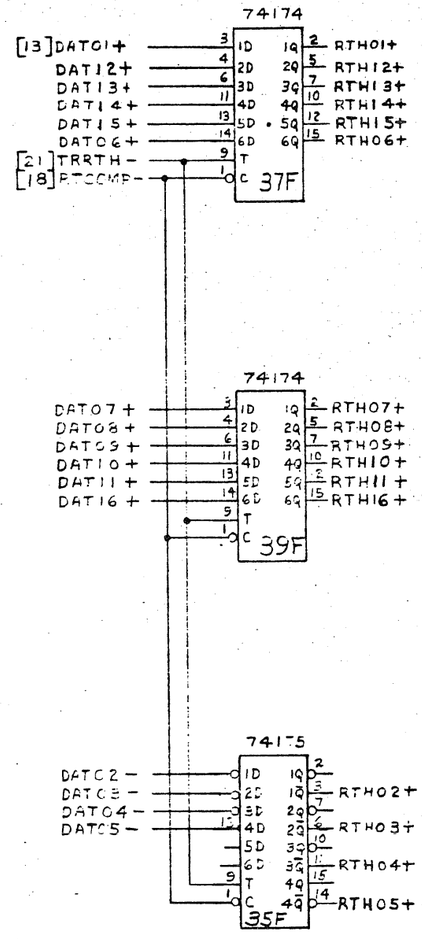
PDF-003

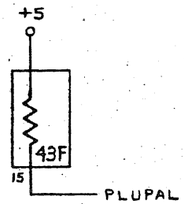
PRIME COMPUTER, INC.



III-14

MATERIAL	DWN A. Bryan 1/17/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC DMX INTERRUPT RAM
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 13 OF	SIZE C	DWG. NO. LBD1528

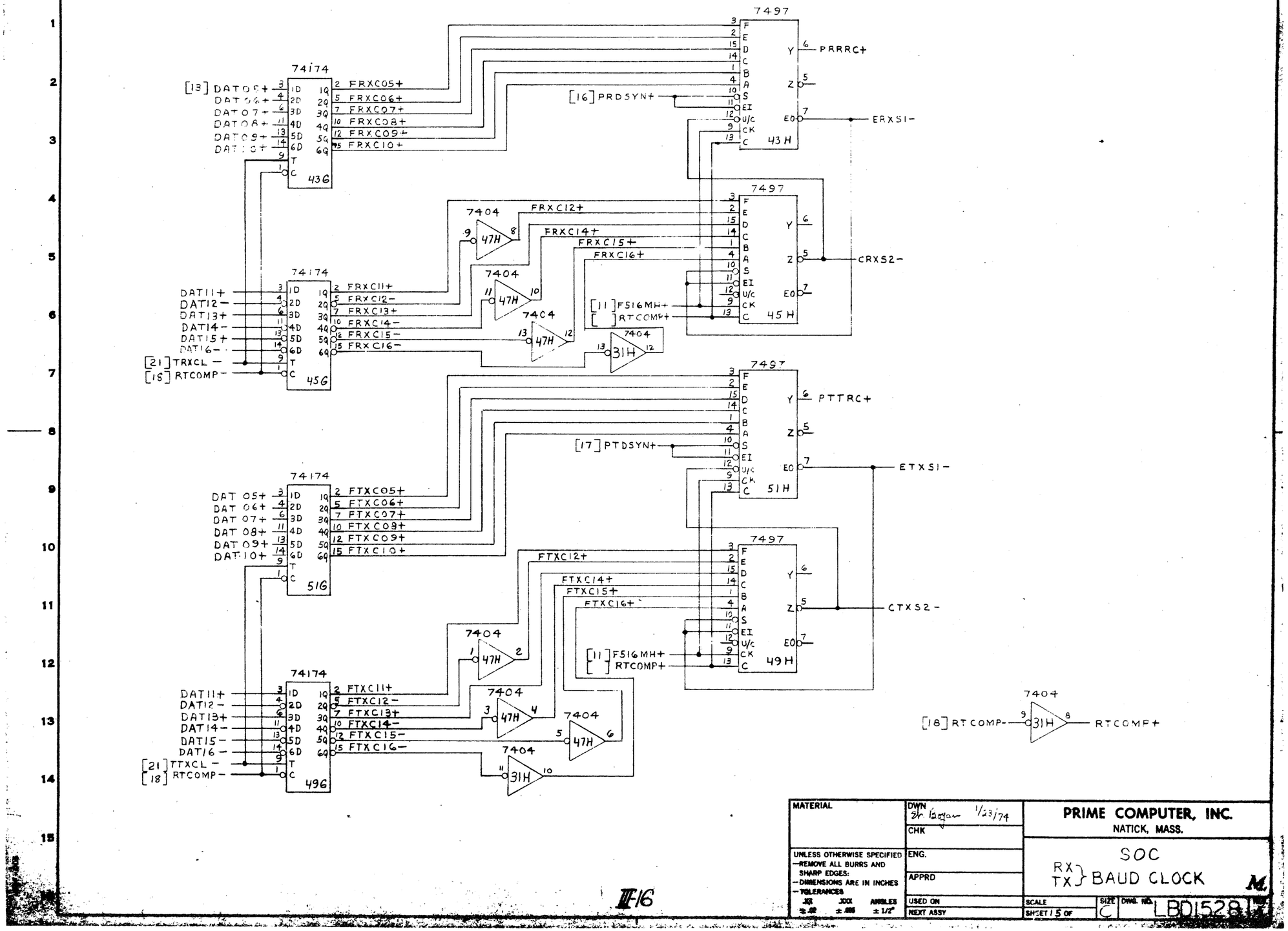




MATERIAL	DWN K Byam 1/23/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	SOC RT HOLDING REG M.
	APPRD	
	USED ON	SCALE — SIZE C DWG. NO. LBD1528 REV. A
	NEXT ASSY	SHEET 14 OF

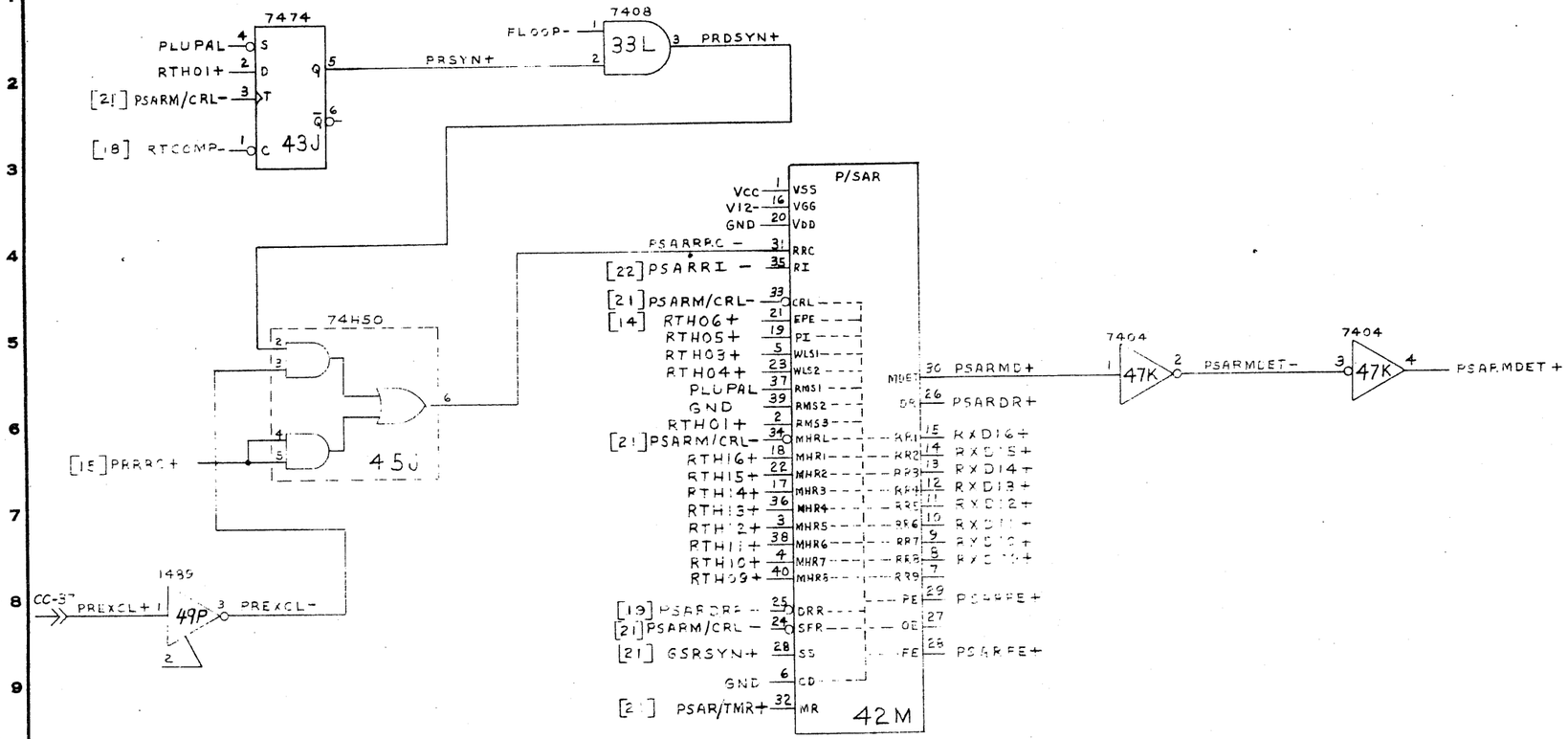
PDF-003

PRIME COMPUTER, INC.



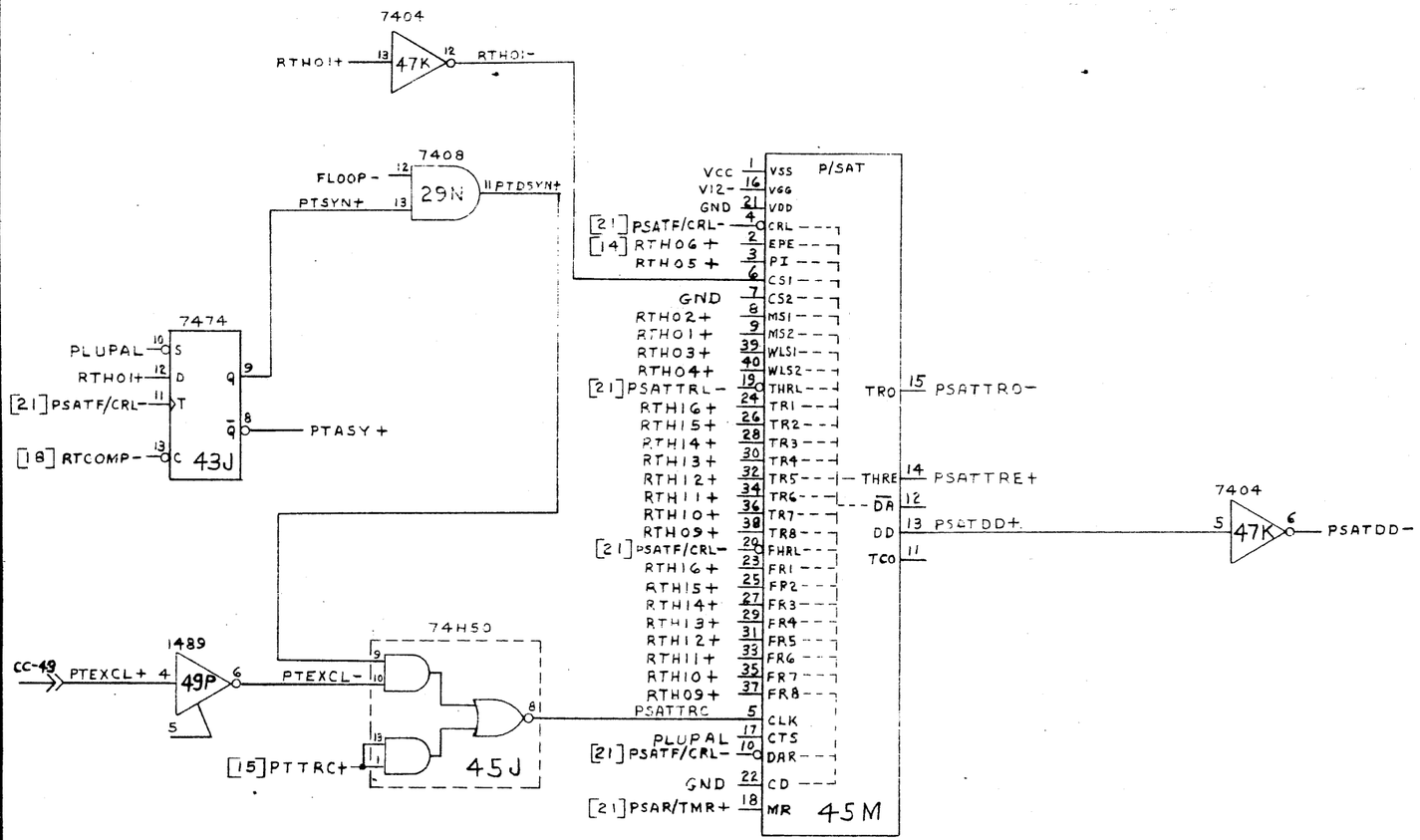
MATERIAL	DWN Sr Bogan 1/23/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	SOC RX/TX BAUD CLOCK	
	APPRD		
	USED ON / NEXT ASSY	SCALE	SIZE C DWG. NO. LBD1528
		SHEET 15 OF	

II-16



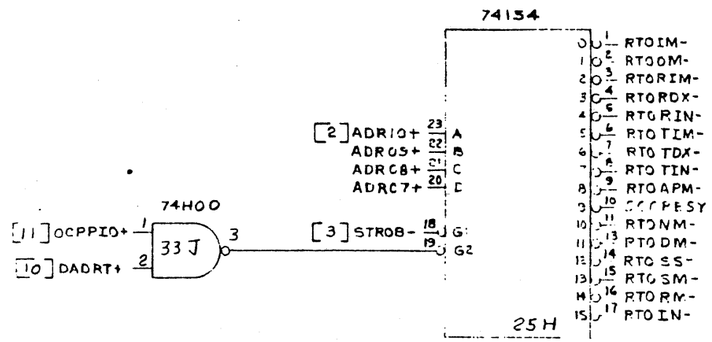
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	SOC PSAR
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 16 OF
		SIZE C / DWG. NO. LBD1528 A

PDF-003



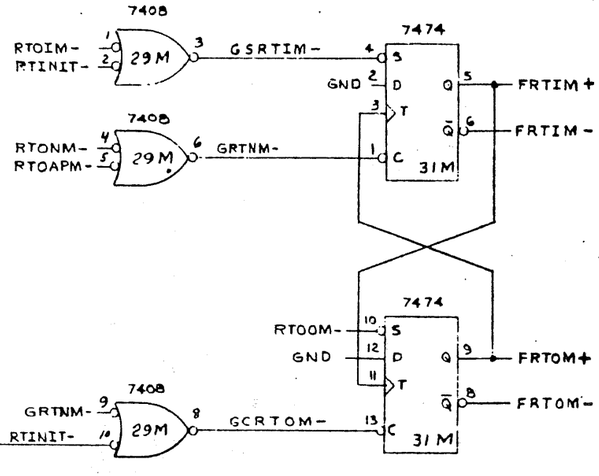
III-18

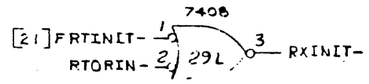
MATERIAL	DWN H. Boyan 1/24/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX .XXX ANGLES ± .02 ± .005 ± 1/2°	ENG.	SOC P SAT
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SHEET 17 OF
		SIZE C DWG. NO. LBD1528 REV. A

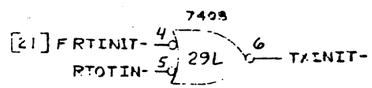


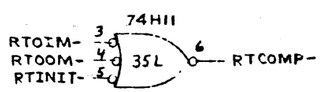
OCP

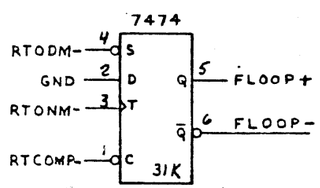
SET	INPUT MODE
	OUTPUT MODE
	RX INTERRUPT MODE
	RX DMX MODE
	RX INITIALIZE
	TX INTERRUPT MODE
	TX DMX MODE
	TX INITIALIZE
	A' MODE
	— DIAGNOSTIC SYNC
	NORMAL MODE
	DIAGNOSTIC
	SEARCH FOR SYNC
	SET RT INTERRUPT MODE
	RESET RT INTERRUPT MODE
	RT INITIALIZE

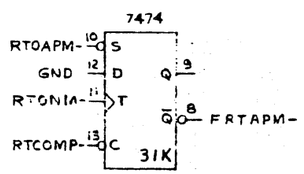


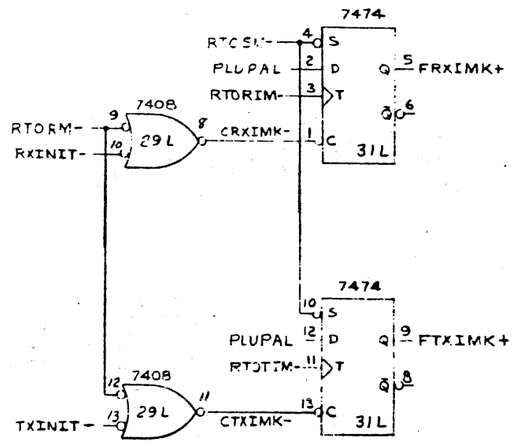




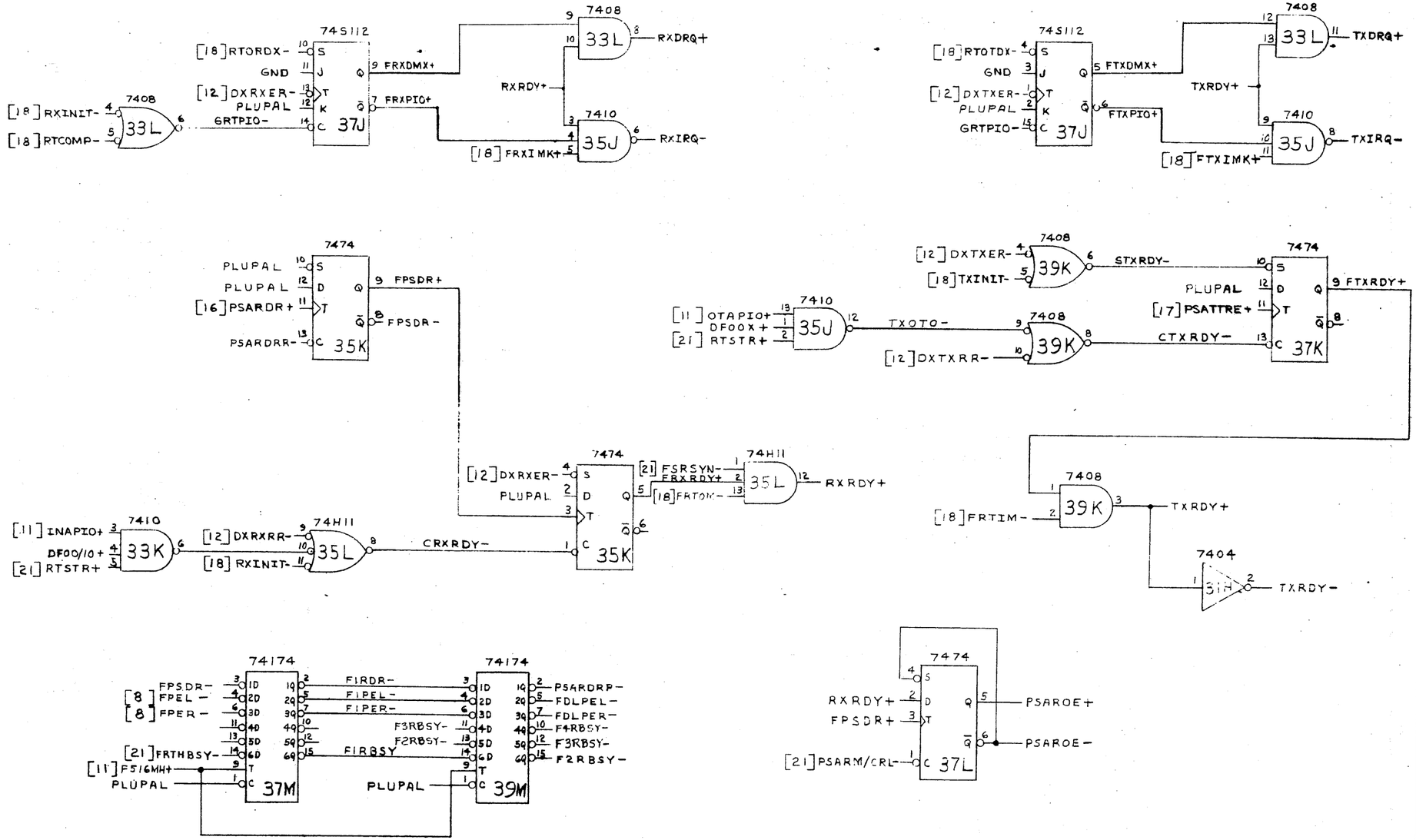




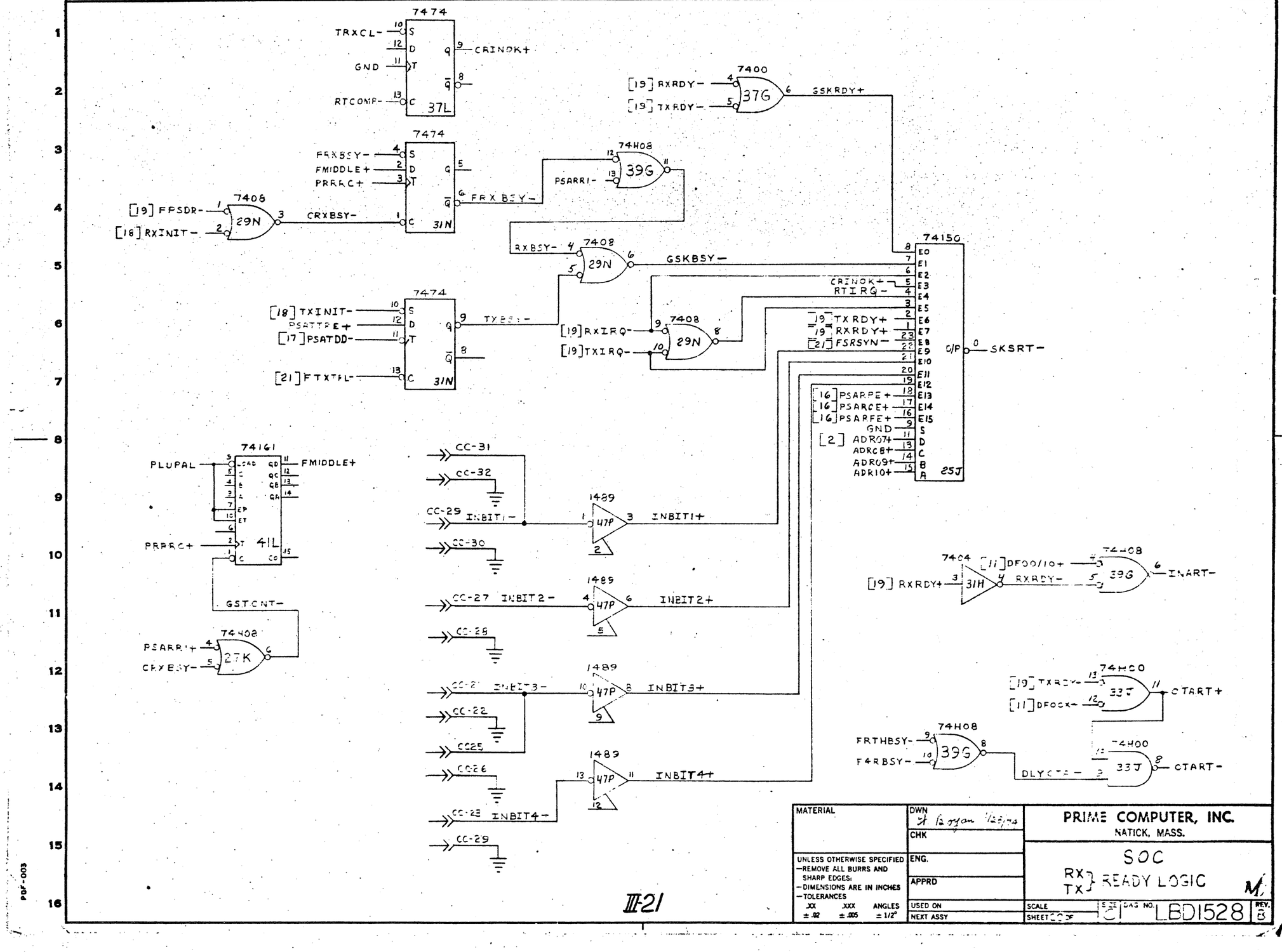




MATERIAL	DWN D.F.C 1-25-74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	SOC RX/TX I/O CONTROL	
	APPRD		
	USED ON	SCALE — SIZE C DWG. NO. LBD1528	REV. A
	NEXT ASSY	SHEET 18 OF	

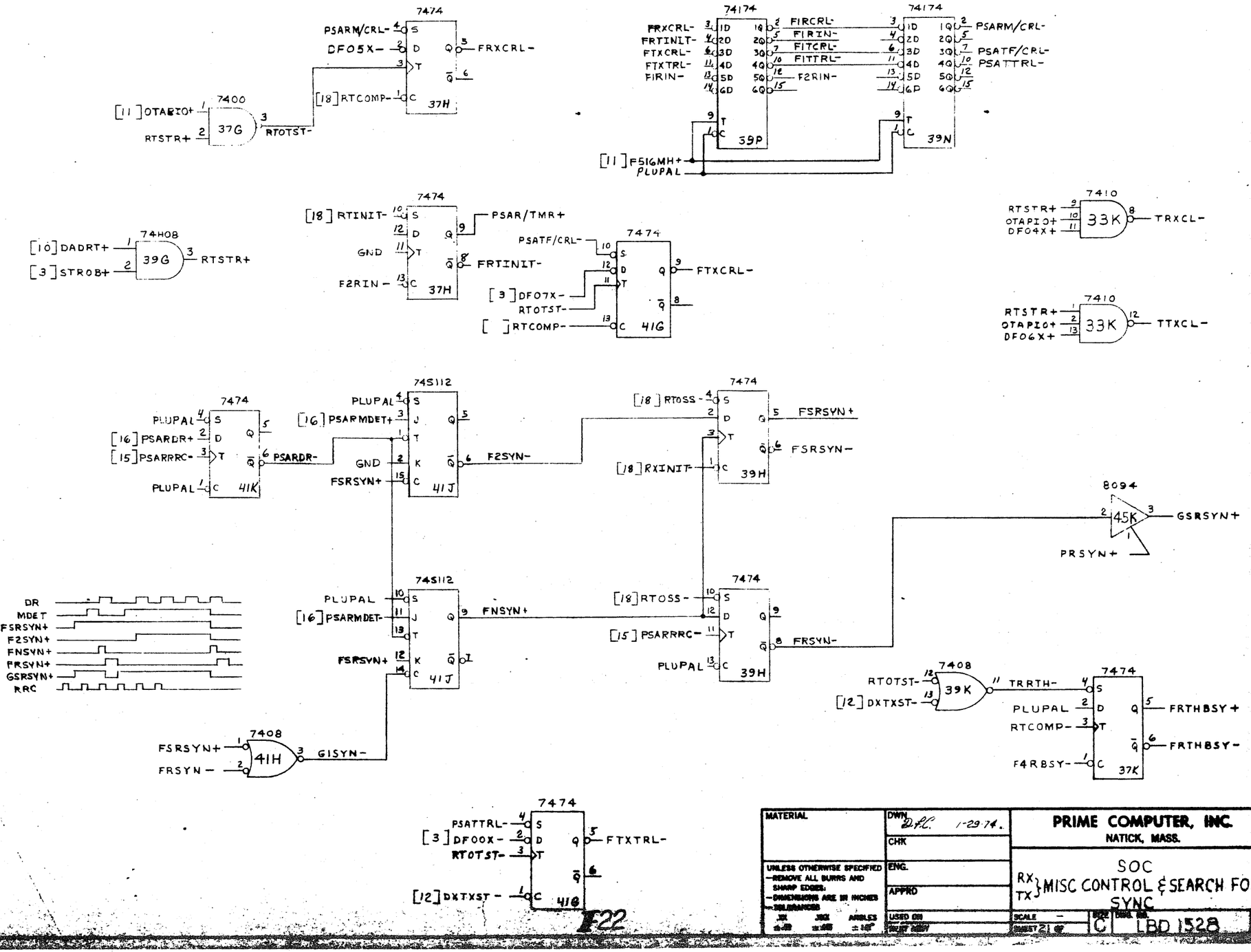


MATERIAL	DWN D.F.C. 1-25-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC RX/TX READY, IRQ, DRQ
	ENG.	
	APPRD	
	USED ON	SCALE — SIZE C DWG. NO. BD1528 REV. A
	NEXT ASSY	SHEET 19 OF

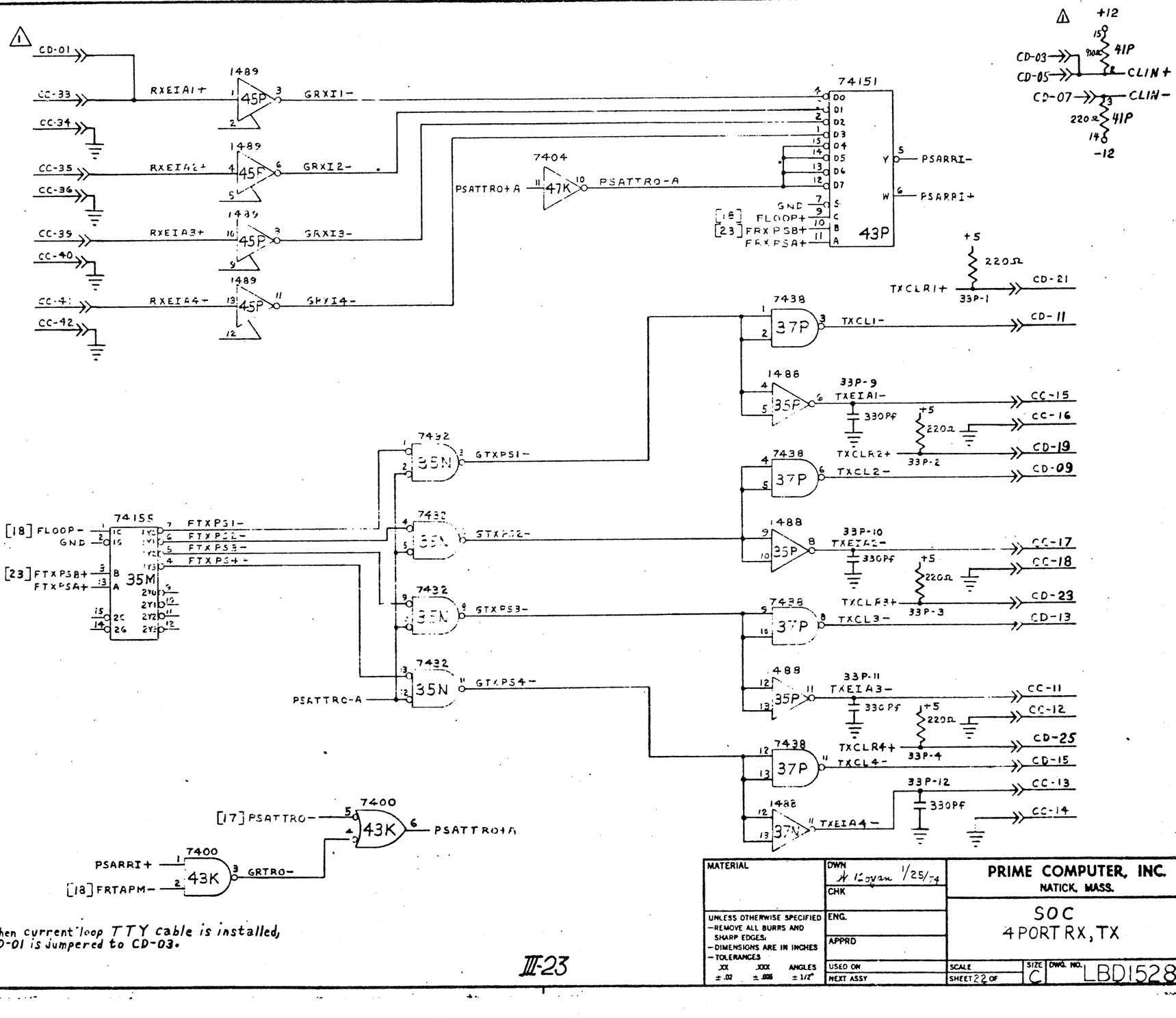


MATERIAL	DWN H Bryan 12/9/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC RX/TX READY LOGIC	
	APPRD		
	USED ON	SCALE	SIZE D DWG NO. LBD1528 REV. B
	NEXT ASSY	SHEET 20 OF 31	

PRF-003

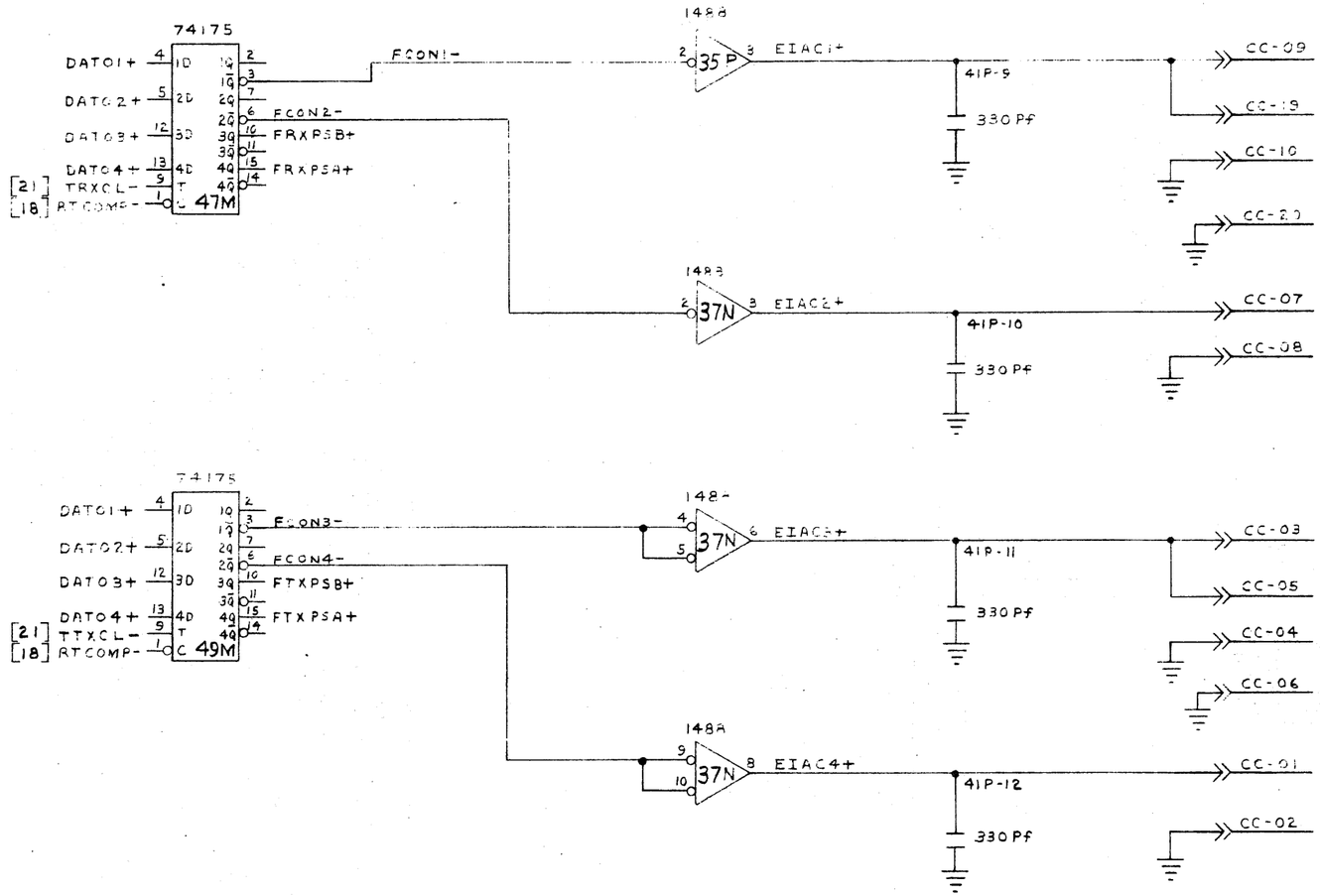


MATERIAL	DWN D.F.C. 1-29-74.	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX .XXX ANGLES	CHK	SOC RX/TX } MISC CONTROL & SEARCH FOR SYNC
	ENG.	
	APPRD	
	USED ON NEXT ASSY	SCALE — SHEET 21 SIZE C DWG NO. LBD 1528

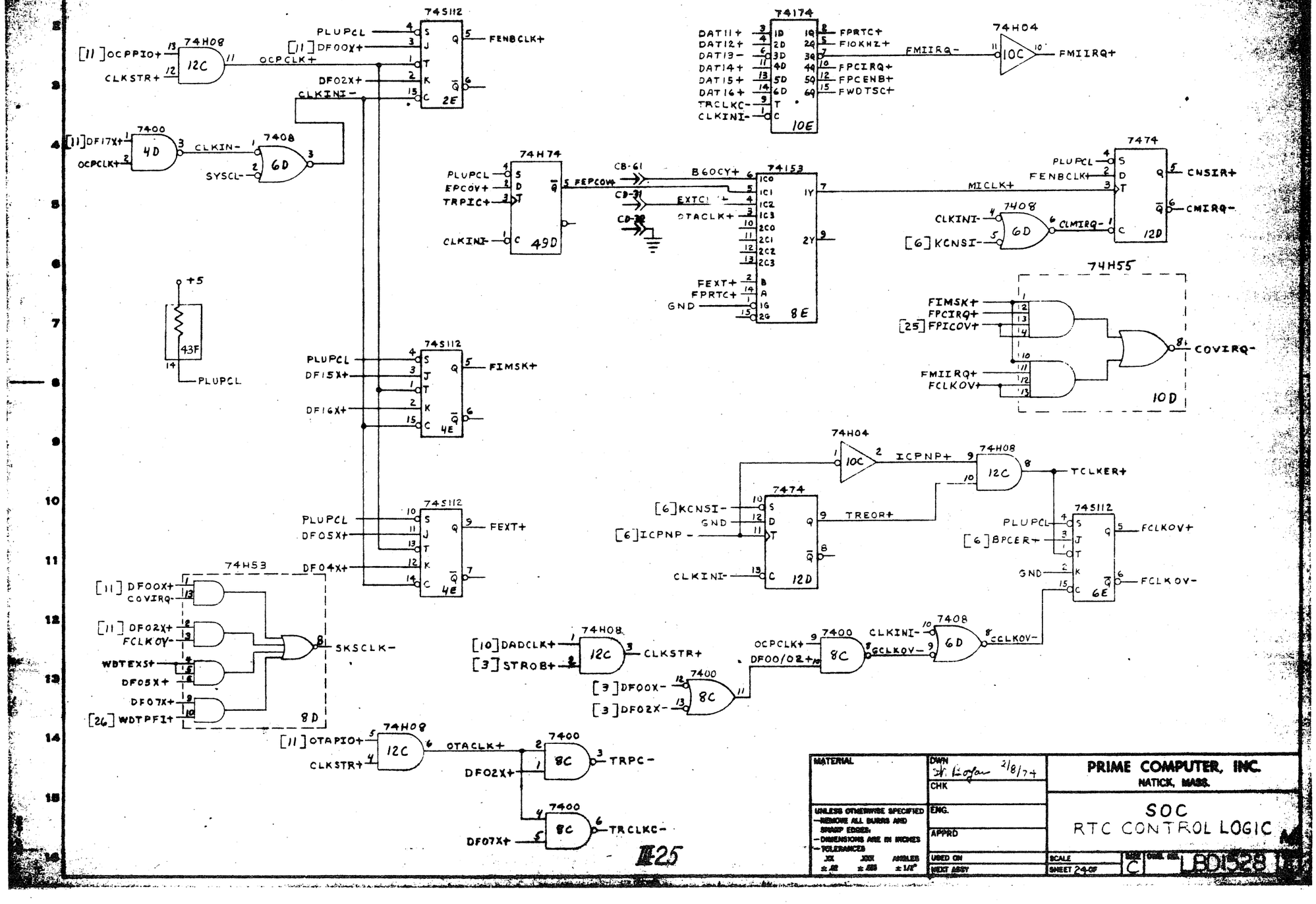


⚠ When current loop TTY cable is installed, CD-01 is jumpered to CD-03.

MATERIAL	DWN N Kenyan 1/25/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED – REMOVE ALL BURRS AND SHARP EDGES; – DIMENSIONS ARE IN INCHES – TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	SOC 4 PORT RX, TX
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 22 OF
		SIZE C / DWG. NO. LBD1528 / REV. M

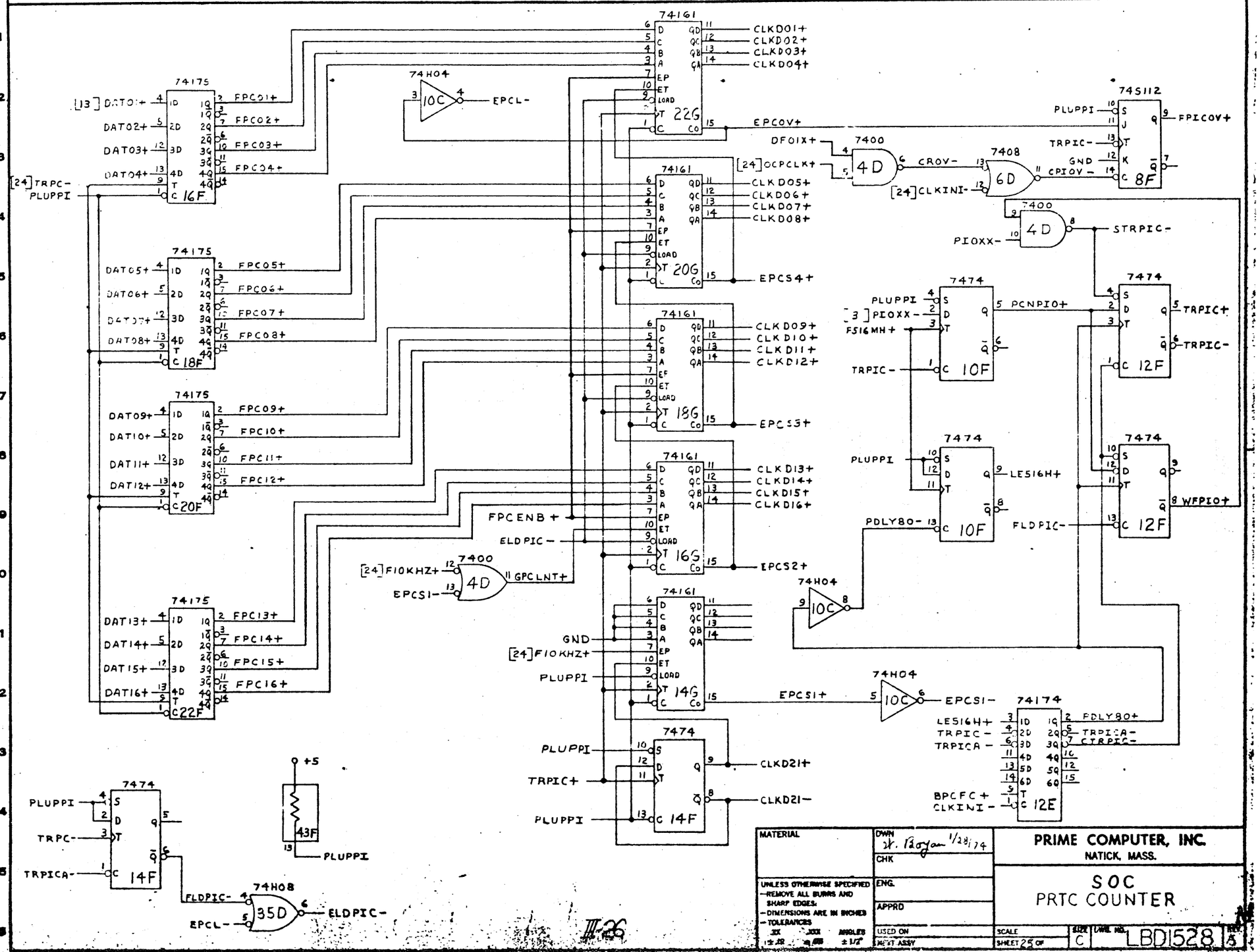


MATERIAL	DWN J. Boyan 3/28/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX .XXX ANGLES ±.02 ±.005 ±1/2°	ENG.	SOC CON BITS 1-4
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 23 OF
		SIZE C / DWG. NO. LBD1528



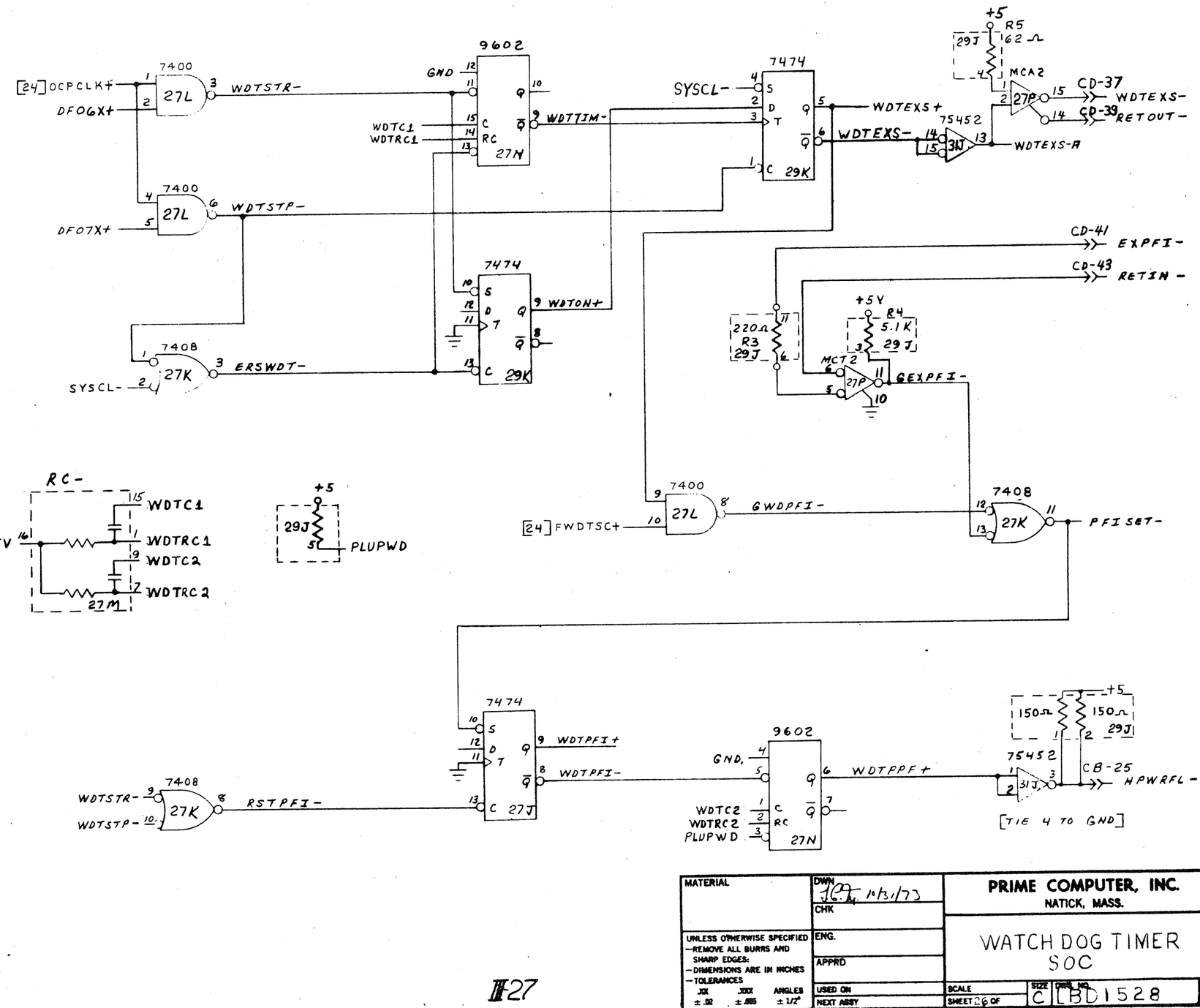
MATERIAL	DWN H. Logan 2/8/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES. –DIMENSIONS ARE IN INCHES –TOLERANCES .XX .XXX ANGLES ±.02 ±.005 ±1/2°	ENG.	SOC RTC CONTROL LOGIC
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SHEET 24 OF
		SIZE C DWG. NO. LBD1528

II-25



MATERIAL	DWN W. Regan 1/28/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX .XXX ANGLES ± .02 ± .005 ± 1/2°	CHK	SOC PRTC COUNTER
	ENG.	
	APPRD	
USED ON NEXT ASSY	SCALE	SIZE C — DWG. NO. LBD1528 — REV. A
	SHEET 25 OF	

PRIME COMPUTER, INC.



MATERIAL	DWN JCG 10/31/73	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	WATCH DOG TIMER SOC
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 26 OF
		SIZE C DWG. NO. LBD1528 REV. A

II-27

300-694

74157 02M: [13] DAT01+ BIOD09+ DAT02+ BIOD10+ DAT03+ BIOD11+ DAT04+ BIOD12+; [28] BIENLB-; GBIDO1+ GBIDO2+ GBIDO3+ GBIDO4+
74175 02N: BPIDO1+ BPIDO1- BPIDO2+ BPIDO2- BPIDO3+ BPIDO3- BPIDO4+ BPIDO4-
74H01 02P: BIODO1+ BIODO2+ BIODO3+ BIODO4+; CF-1 CF-3 CF-5 CF-7; 10P; +5

74157 04M: DATO5+ BIOD13+ DATO6+ BIOD14+ DATO7+ BIOD15+ DATO8+ BIOD16+; [28] BIENLB-; GBIDO5+ GBIDO6+ GBIDO7+ GBIDO8+
74175 04N: BPIDO5+ BPIDO5- BPIDO6+ BPIDO6- BPIDO7+ BPIDO7- BPIDO8+ BPIDO8-
74H01 04P: BIODO5+ BIODO6+ BIODO7+ BIODO8+; CF-9 CF-11 CF-13 CF-15; 10P; +5
FBIOML+

74157 06M: DATO9+ BIOD01+ DAT10+ BIOD02+ DAT11+ BIOD03+ DAT12+ BIOD04+; GND; GBIDO9+ GBIDO1+ GBIDO1+ GBIDO1+
74175 06N: BPIDO9+ BPIDO9- BPIDO1+ BPIDO1- BPIDO1+ BPIDO1+ BPIDO1+ BPIDO1-
74H01 06P: BIODO9+ BIODO1+ BIODO1+ BIODO1+; CF-17 CF-19 CF-21 CF-23; 10P; +5

74157 08M: DAT13+ BIOD05+ DAT14+ BIOD06+ DAT15+ BIOD07+ DAT16+ BIOD08+; GND; GBIDO1+ GBIDO1+ GBIDO1+ GBIDO1+
74175 08N: BPIDO1+ BPIDO1- BPIDO1+ BPIDO1- BPIDO1+ BPIDO1+ BPIDO1+ BPIDO1-; [28] TBPIR-
74H01 08P: BIODO1+ BIODO1+ BIODO1+ BIODO1+; CF-25 CF-27 CF-29 CF-31; 10P 12P; +5
FBIOMR+

7408 41H: CBPIDR- [28] SYSCL-; BIRRSY-

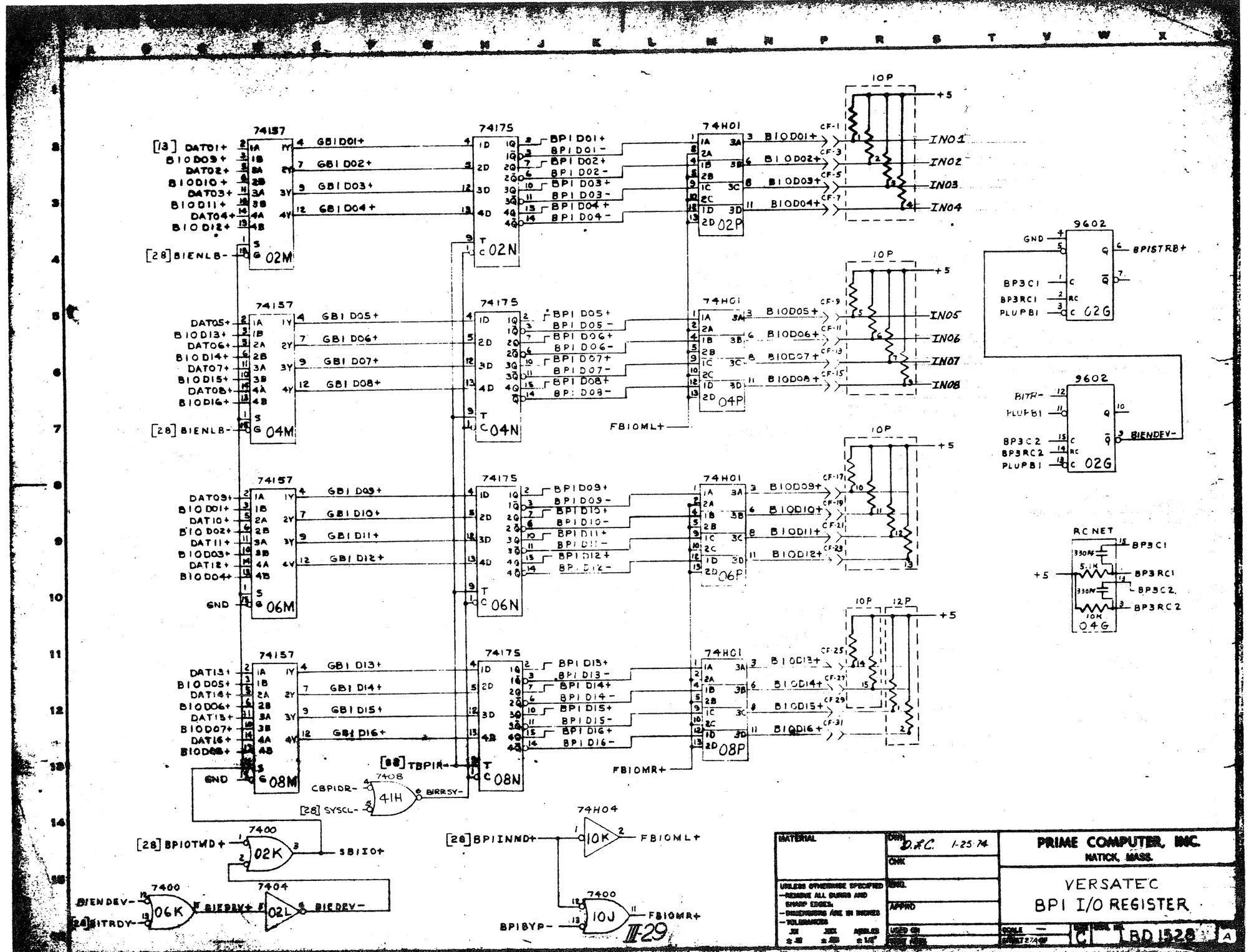
7400 02K: [28] BPIOTMD+; SBIIO+
74H04 10K: [28] BPIINMD+; FBIOML+
7400 06K: BIENDEV- [28] BITRDY-; BIEDEV+
7404 02L: BIEDEV+; BIEDEV-
7400 10J: BPIBYP-; FBIOMR+

9602 02G: GND; BPISTRB+; BP3C1 BP3RC1 PLUPB1
9602 02G: BITR- PLUPB1; BP3C2 BP3RC2 PLUPB1; BIENDEV-

RC NET 04G: +5; 330PF 5.1K 330PF 10K; BP3C1 BP3RC1 BP3C2 BP3RC2

PDF-003

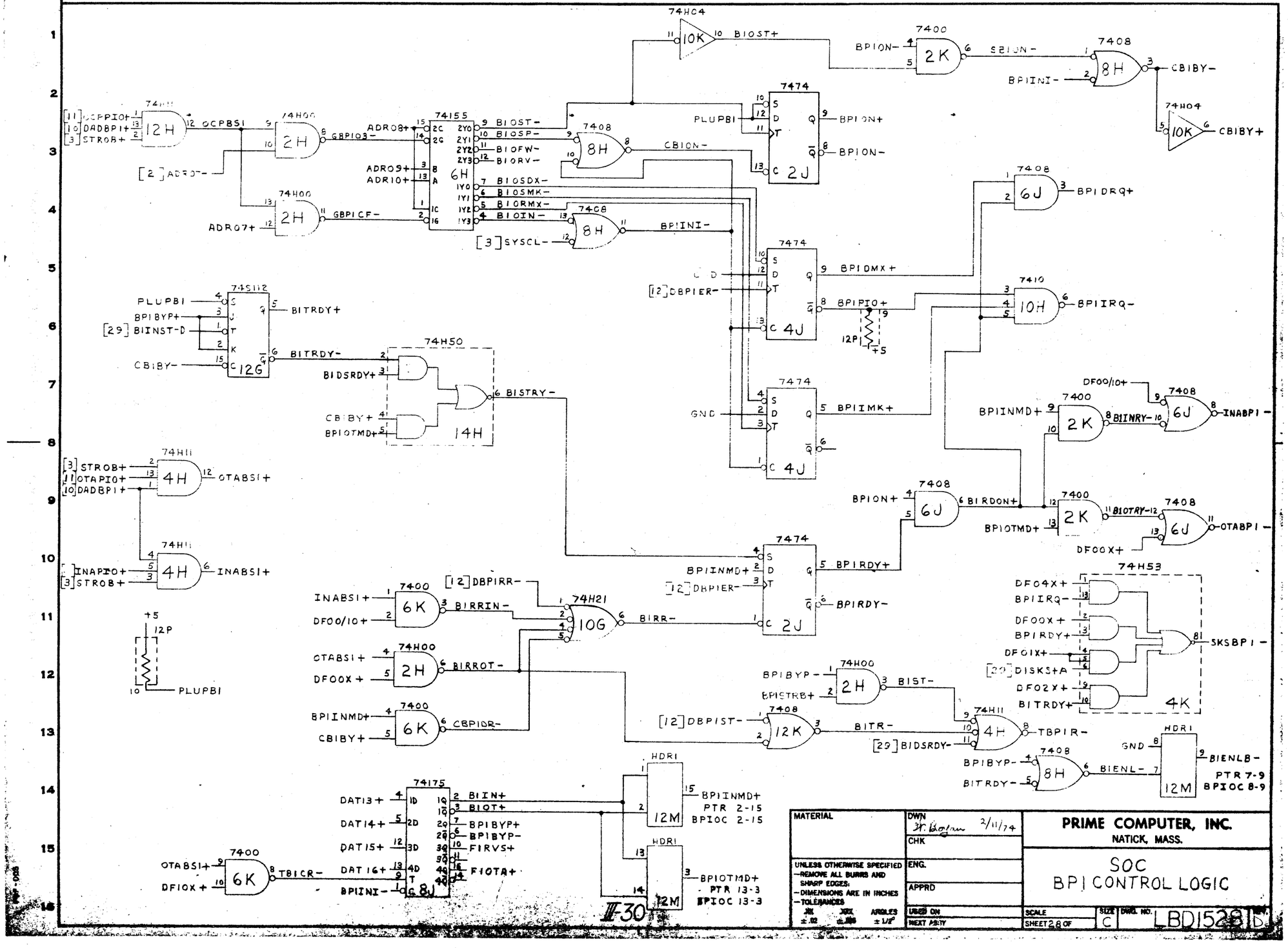
MATERIAL	DWN D.F.C. 1-25-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC BPI I/O REGISTER	
	ENG.		
	APPRD		
USED ON / NEXT ASSY	SCALE — SHEET 27 OF	SIZE C DWG. NO. LBD1528	REV B



MATERIAL	DWN D.R.C. 1-25-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.010 ANGLES ±1/2°	CHK	VERSATEC BPI I/O REGISTER
	ENG.	
	APPRD	
	USED ON	SCALE — SHEET 2 OF 4 SIZE C DWG. NO. BD1528 REV A

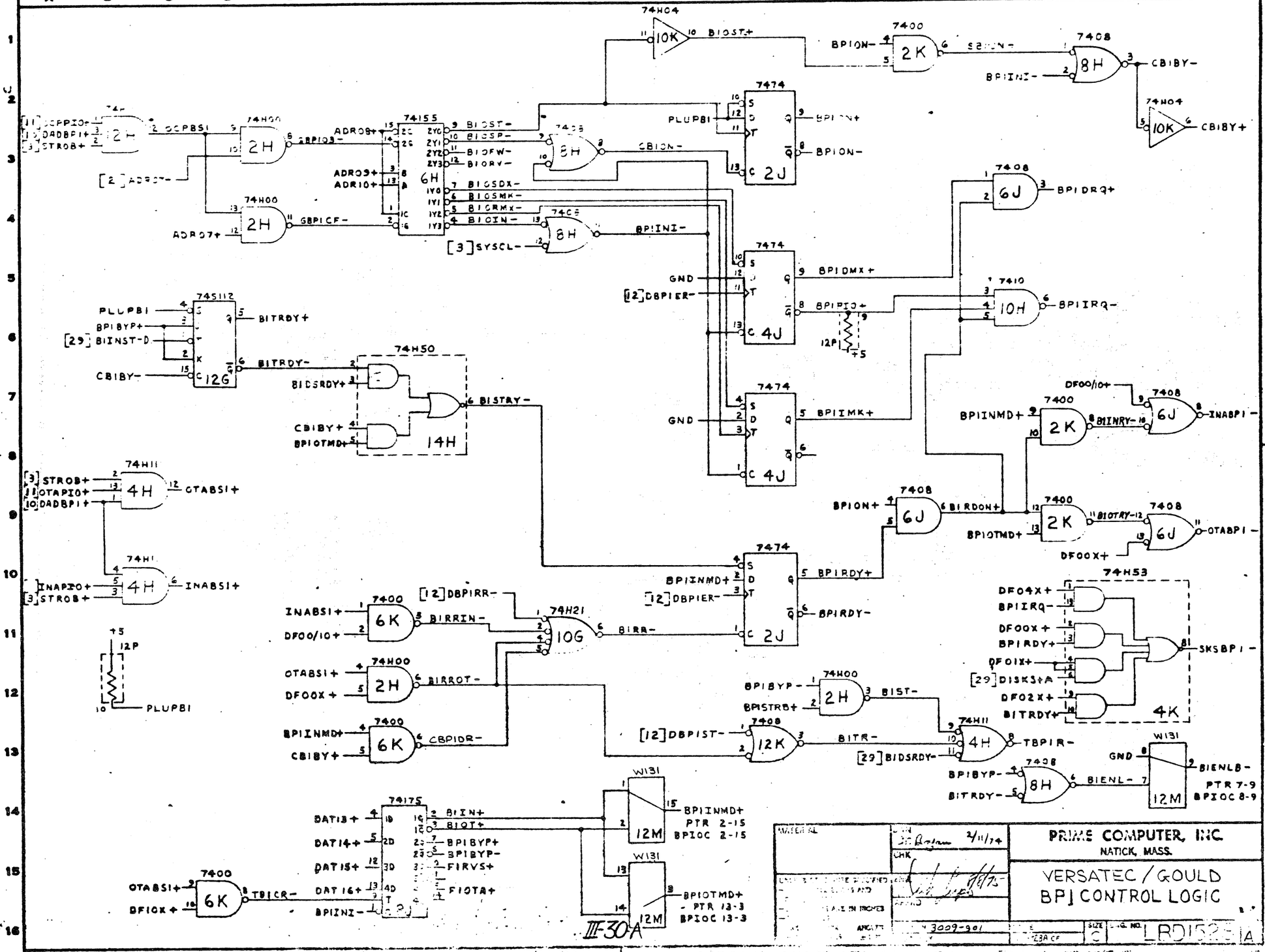
II-29

PRIME COMPUTER, INC.



MATERIAL	DWN H. Bogan 2/11/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC BPI CONTROL LOGIC	
	APPRD		
	USED ON NEXT ASSY	SCALE SHEET 28 OF	SIZE C DWG. NO. LBD1528 REV. D

PRIME COMPUTER, INC.



MATERIAL	DRN J.C. Bogan 2/11/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	VERSATEC / GOULD BPI CONTROL LOGIC	
	APPD	3009-901	SIZE C — DWG NO. LRD1525-1A

POP-025

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

DISTRB 7414 10N DISTRB- 7414 10N DISTRB+ HDR1 SELECT STRB LEVEL 10M DISTRB+A
PTR 1-15 BPIOC 1-15

DISTRB+ DISTRB- HDR1 SELECT STROBE EDGE 10L
PTR 2-15 BPIOC 1-15

9602 4L BIINST+A BIINST+D BIINST-D BIC1 BIRC1 BPION+ BIC2 BIRC2
PTR 100 N SEC BPIOC 3 μSEC
PTR 100 N SEC BPIOC 100 N SEC

DIRDY 7414 10N DIRDY- 7414 10N DIRDY+ HDR1 SELECT RDY LEVEL 10M DIRDY+A
PTR 14-3 BPIOC 14-3

DISTRB+B 7486 12N
BPIOTMD+ 7486 12N BIST+

BIDSRDY+ BITRDY+ 7400 10J BISTDLY+ BISP- HDR1 10L BISETMV+
PTR 13-3 BPIOC 13-3

BPIRDY- FIIRDY- 7406 41H EDIRDY+ BISETMV+ DIRDY+A BPION+ 7420 12J BIDRDY-

GND BIDRDY- BIC3 BIRC3 PLUPBI 9602 3L BIDRDY-D
PTR 1 M SEC BPIOC 3 μSEC

PLUPBI BPION+ 7474 8K BIDRVF+ HDR1 SELECT DRIVE LEVEL PULSE 10L BIDRIVE+
PTR 5-12 BPIOC 4-12

7400 10J BIDF- 7404 2L BIDF+A HDR1 SELECT MVF LVL 10M DIMVF
CF-35 PTR 5-12 BPIOC 5-12

7400 10J BIDR- 7404 2L BIDR+A HDR1 SELECT MVF LVL 10M DIMVR
CF-43 PTR 11-6 BPIOC 11-6

[28] CBIBY- BIDSRDY- 7408 12K BIDDR-

9602 PLUPBI BIC4 BIRC4 PLUPBI 8L BIDRVS+
PTR 3 μSEC BPIOC 3 μSEC

BIRC3+

74174 BIST+ BISTDI+ BISTD2+ F5MHZ+ PLUPBI 29P BISTDI+ BISTD2+ BISTDLY+

7474 BIORV- GND BIOFW- [28] BPIINI- 8K FIBCK+ FIFWL+ HDR1 SELECT FWD= RVS 10L
PTR 10-6 BPIOC 11-6

+5 12P DISKS CF-33 74.4 10N DISKS- 74.4 10N DISKS+ HDR1 SELECT SKS LEVEL 12M DISKS+A
PTR 5-12 BPIOC 5-12

RCNET +5 BIC1 BIRC1 BIC2 BIRC2 BIC3 BIRC3 BIC4 BIRC4 6L

74H11 29F BISTRY- BIST- BITR- GND FUFI- BPIOTMD+ 7474 27J FIIRDY-

[28] FIOTA+ 7404 2L FIOTA- 7404 2L FIOTA+ HDR1 SELECT DTA LVL 12M DIOTA
CF-39 PTR NONE BPIOC 11-6

II-31

MATERIAL	DWN N. Rojan 2/7/74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ± 1/2°	CHK	SOC BPI DEVICE INTERFACE	
	ENG.		
	APPRD		
	USED ON NEXT ASSY	SCALE SHEET 29 OF	SIZE C DWG. NO. LBD1528 REV D

P&F-603

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

READY DISTRB — CF-41 — 7414 10N — DISTRB− — 7414 10N — DISTRB+ — W14 SELECT STRB LEVEL 10M — DISTRB+A — PTR 1-15 BPIOC 1-15

DISTRB+ / DISTRB− — W103 SELECT STROBE EDGE 10L — PTR 2-15 BPIOC 1-15

9602 4L: GND 4, BINST+A 5, BICI 1, BIRCI 2, BPION+ 3, C, RC, CD; Q 6 BINST+D, Q̄ 7 BINST-D — PTR 100 N SEC BPIOC 3 μSEC

9602 4L: GND 12, BIC2 15, BIRC2 14, BPION+ 13, C, RC, CD; Q 10 BIDSRDY+, Q̄ 9 BIDSRDY− — PTR 100NSEC BPIOC 100NSEC

READY DIRDY — CF-37 — 7414 10N — DIRDY− — 7414 10N — DIRDY+ — W14 SELECT RDY LEVEL 10M — DIRDY+A — PTR 14-3 BPIOC 14-3

DISTRB+B — 7486 12N — BPIOTMD+ — 7486 12N — BIST+

BIDSRDY+ / BITRDY+ — 7400 10J — BISTDLY+ — W103 B SP-14 10L — BISETMV+ — PTR 3-3 BPIOC 13-3

BPIRDY− / FIIRDY− — 7408 41H — BDIRDY+ — BISETMV+ / DIRDY+A / BPION+ — 7420 12J — BIDRDY−

9602 8L: GND 12, BIDRDY− 11, BIC3 15, BIRC3 14, PLUPBI 13, C, RC, CD; Q 10, Q̄ 5 BIDRDY-D — PTR 1 MSEC BPIOC 3 μSEC

PLUPBI / BPION+ — 7474 8K: S 4, D 2, T 3, C 1; Q 5 BIDRVF+, Q̄ 6

W103 SELECT DRIVE LEVEL PULSE 10L: BIDRVF+ 4, BIDRIVE+ 12 — PTR 5-12 BPIOC 4-12

7400 10J: BIDRIVE+ 5 → 4 → 6

BIDF− — 7404 2L — BIDF+A — W14 SELECT M/F L/L 10M — DINVF — CF-35 PTR 5-12 BPIOC 5-12 — PICLK

7400 10J: 10 → 9 → 8

BIDR− — 7404 2L — BIDR+A — W14 SELECT M/F L/L 10M — DINVR — CF-43 — RLTER

[28] CBIBY− / BIDSRDY− — 7408 12K — BIDDR−

5602 8L: PLUPBI 4, BIC4 1, BIRC4 2, PLUPBI 3, C, RC, CD; Q 6 BIDRVS+, Q̄ 7 — PTR 3 μSEC BPIOC 3 μSEC

BIDRV+ / GND / B OFW− / [28] BPIINI− — 7474 8K: S 10, D 12, T 11, C 13; Q 9 FIBCP+, Q̄ 8 FIFWD+

W103 SELECT FNC DVS 10L: FIBCP+ 10, FIFWD+ 11, 6 — PTR 10-6 BPIOC 11-6

[28] FIPVS+

74174 29P: BIST+ 3D, BISTD1+ 4D, BISTD2+ 6D, FSMHZ+ 9 T, PLUPBI 1 C; 1Q 2 BIST+, 2Q 5 BISTD1+, 3Q 7 BISTD2+, 4Q 12 BISTDLY+, 5Q 13, 6Q 15

ONLINE DISKS — CF 33 — +5 — 12P — 7414 10N — DISKS− — 7414 10N — DISKS+ — W131 SELECT DKS LEVEL 12M — DISKS+A — PTR 5-12 BPIOC 5-12

RC1116 6L: +5, BIC1, BIRC1, BIRC2, BIC3, BIRC3, BIC4, BIRC4

[28] BISTRY− / BIST− / BITR− — 74H11 29F: GND 7, FUFI− 12 — 7474 27J: S 4, D 2, T 3, C 1; Q 5, Q̄ 6 FIIRDY− — [28] BPIOTMD+

[28] FIOTA+ — 7404 2L — FIOTA− — 7404 2L — FIOTA+A — W131 SELECT DTA L/L 12Y — DIOTA — CF-39 — PRINT/PLOT — PTR NONE BPIOC 11-6

IF31A

MATERIAL	DWN A Kenyon 2/7/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	VERSATEC BPI DEVICE INTERFACE
	ENG.	
	APPRD	
	USED ON 3009-901 / NEXT ASSY	SCALE / SHEET 24 OF	SIZE C	DWG NO LD 528	REV C

PDF-003

PRIME COMPUTER, INC.

A B C D E F G N J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

RDATA DISTRB — CF-41 — +5 — 12P — 7414 10N — DISTRB- — 7414 10N — DISTRB+ — W187 SELECT STRB LEVEL 10M — DISTRB+A — PTR 1-15 BPIOC 1-15

DIRDY — CF-37 — +5 — 12P — 7414 10N — DIRDY- — 7414 10N — DIRDY+ — W137 SELECT RDY LEVEL 10M — DIRDY+A — PTR 14-3 BPIOC 14-3

DISTRB+ — DISTRB- — W10 SELECT STROBE EDGE 10L — PTR 2-15 BPIOC 1-15

DISTRB+B — 7486 12N — BPIOTMD+ — 7486 12N — BIST+

9602 — GND — BIDRDY- — BIC3 — BIRC3 — PLUPBI — CD 8L — BIDRDY-D — PTR 1 M SEC BPIOC 3 M SEC

PLUPBI — BPION+ — 7474 — BIDRVF+ — W10 SELECT DRIVE LEVEL PULSE 10L — BIDRIVE+ — PTR 5-12 BPIOC 4-12

7400 10J — BIDF- — 7404 2L — BIDF+A — W137 SELECT MVF L/L 10M — DIMVF — GDATA — CF-35 — PTR 5-12 BPIOC 5-12

7400 10J — BIDR- — 7404 2L — BIDR+A — W137 SELECT MVF -/- 10M — DIMVF — CF-43 — PTR 11-6 BPIOC 11-6

[28] CBIBY- — BIDSRDY- — 7408 12K — BIDR-

9602 — PLUPBI — BIC4 — BIRC4 — PLUPBI — CD 8L — BIDRVS+ — PTR 3 M SEC BPIOC 3 M SEC

BIRVS+

9602 — GND — BIINST+A — BICI — BIRCI — BPION+ — CD 4L — BIINST+D — BIINST-D — PTR 100 N SEC BPIOC 3 M SEC

9602 — GND — BIC2 — BIRC2 — BPION+ — CD 4L — BIDSADY+ — BIDSRDY- — PTR 100 N SEC BPIOC 100 N SEC

BIDSRDY+ — BITRDY+ — 7400 10J — BISTDLY+ — BISP- — W10 10L — BISETMV+ — PTR 13-3 BPIOC 13-3

BPIRDY- — FIIRDY- — 7408 41H — EDIRDY+ — BISETMV+ — DIRDY+A — BPION+ — 7420 12J — BIDRDY-

74174 — BIST+ — BISTDI+ — BISTD2+ — FSMHZ+ — PLUPBI — 29P — BISTDI+ — BISTD2+ — BISTDLY+

7474 — BIORV- — GND — BIOFW- — [28] BPIINI- — C 8K — FIBCK+ — FIFWD+

W10 SELECT FWD=RVS 10L — PTR 10-6 BPIOC 11-6 — [28] FIRVS+

SBUSY DISKS — CF-33 — +5 — 12P — 7414 10N — DISKS- — 74-4 10N — DISKS+ — W131 SELECT SXS LEVEL 12M — DISKS+A — PTR 5-12 BPIOC 5-12

RC11B — +5 — BIC1 — BIRC1 — BIC2 — BIRC2 — BIC3 — BIRC3 — BIC4 — BIRC4 — 6L

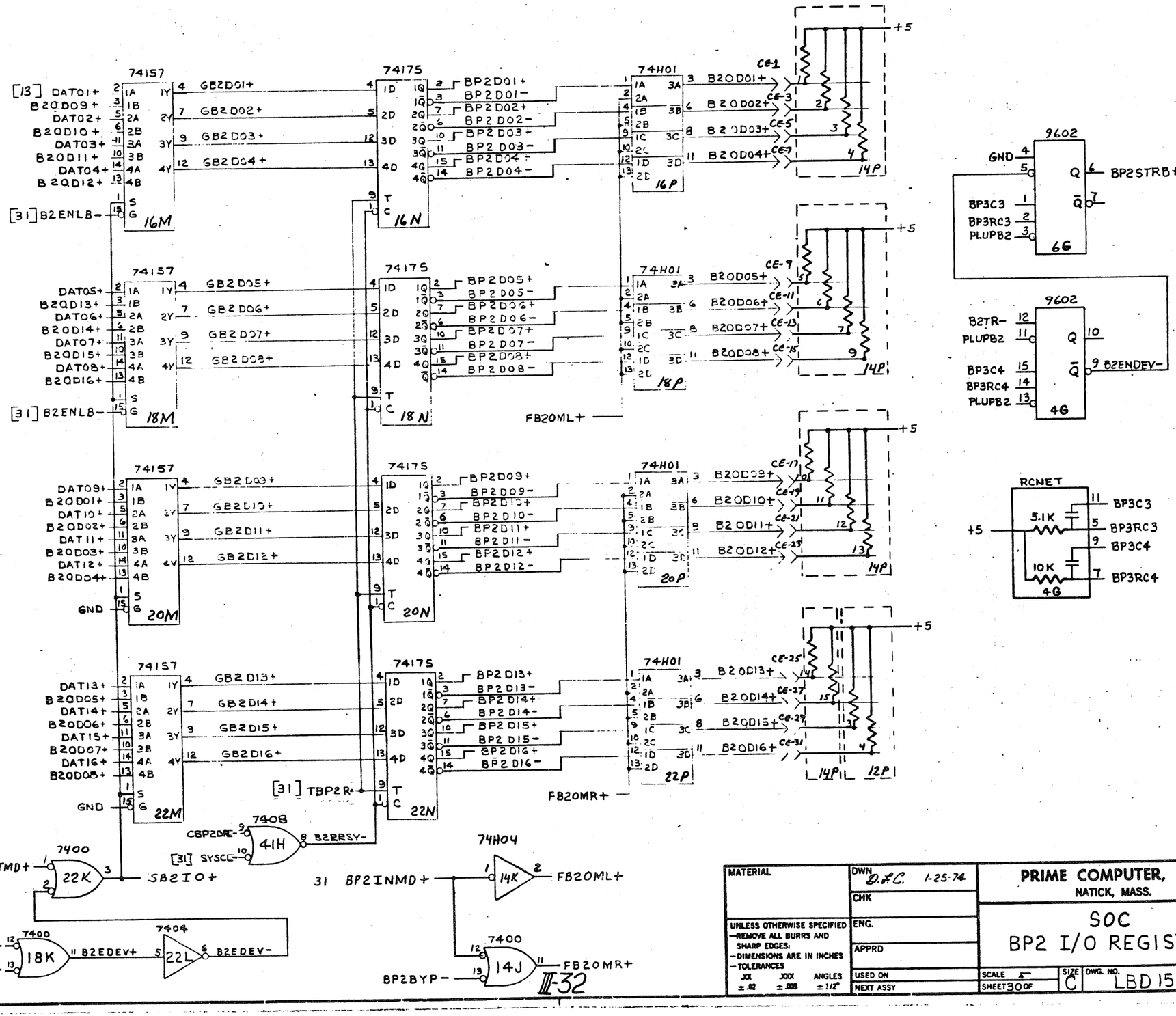
[28] BISTRY- — BIST- — BITR- — 74H11 29F — GND — FIJFI- — 7474 — S D T C — FIIRDY- — [28] BPIOTMD+ — 27J

74174 — BIST+ — BISTDI+ — BISTD2+ — FSMHZ+ — PLUPBI — 29P — BISTDI+ — BISTD2+ — BISTDLY+

7404 2L — FIOTA+ — FIOTA- — 7404 2L — FIOTA+A — W131 SELECT FTA LVL 12M — FIOTA — CF-39 — PTR NONE BPIOC 11-6

II-31-B

MATERIAL	DWN Paul Beatrice 7-28-75	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	GOULD BPI DEVICE INTERFACE	
	ENG Dick Lyon 8/8/75		
	APPRD		
	USED ON 50018-001	SCALE	SIZE C DWG. NO. LBD1528 REV. B
	NEXT ASSY	SHEET 29 B OF	



MATERIAL	DWN D.F.C. 1-25-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC BP2 I/O REGISTEP	M
	ENG.		
	APPRD		
	USED ON / NEXT ASSY	SCALE — SHEET 30 OF	SIZE C DWG. NO. LBD1528 REV. B

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74157 16M

[13] DAT01+ B20D09+ DAT02+ B20D10+ DAT03+ B20D11+ DAT04+ B20D12+ [31] B2ENLB-

GB2D01+ GB2D02+ GB2D03+ GB2D04+

74175 16N

BP2D01+ BP2D01- BP2D02+ BP2D02- BP2D03+ BP2D03- BP2D04+ BP2D04-

74157 18M

DAT05+ B20D13+ DAT06+ B20D14+ DAT07+ B20D15+ DAT08+ B20D16+ [31] B2ENLB-

GB2D05+ GB2D06+ GB2D07+ GB2D08+

74175 18N

BP2D05+ BP2D05- BP2D06+ BP2D06- BP2D07+ BP2D07- BP2D08+ BP2D08-

74157 20M

DAT09+ B20D01+ DAT10+ B20D02+ DAT11+ B20D03+ DAT12+ B20D04+ GND

GB2D09+ GB2D10+ GB2D11+ GB2D12+

74175 20N

BP2D09+ BP2D09- BP2D10+ BP2D10- BP2D11+ BP2D11- BP2D12+ BP2D12-

74157 22M

DAT13+ B20D05+ DAT14+ B20D06+ DAT15+ B20D07+ DAT16+ B20D08+ GND

GB2D13+ GB2D14+ GB2D15+ GB2D16+

74175 22N

BP2D13+ BP2D13- BP2D14+ BP2D14- BP2D15+ BP2D15- BP2D16+ BP2D16-

[31] TBP2R-

7408 41H

CBP2DR- [31] SYSCLR- B2RRSY-

7400 22K

[31] BP20TMD+ SB2IO+

7400 18K

B2ENDEV- [31] B2TRDY- B2EDEV+

7404 22L

B2EDEV-

74H04 14K

31 BP2INMD+ FB20ML+

7400 14J

BP2BYP- FB20MR+

74H08 22P

FB20MR+ B20D13+ B20D14+ B20D15+ B20D16+

CLEAR RFEED RESET REQTR

14P 12P

+5 CE-1 B20D01+ CE-3 B20D02+ CE-5 B20D03+ CE-7 B20D04+ 14P

+5 W133 7 3 B20D05+ CE-7 6 B20D06+ CE-11 8 B20D07+ CE-13 11 B20D08+ CE-15 18P 14P

+5 B20D09+ CE-17 B20D10+ CE-19 B20D11+ CE-21 B20D12+ CE-23 14P

VERSATEC ONLINE READY NO PAPER

+5 CE-25 B20D13+ CE-27 B20D14+ CE-29 B20D15+ CE-31 B20D16+ 14P 12P

CLEAR RFEED RESET REQTR

9602 66

GND BP3C3 BP3RC3 PLUPB2 BP2STRB+

9602 46

B2TR- PLUPB2 BP3C4 BP3RC4 PLUPB2 B2ENDEV-

RC107 46

+5 3.1K 10K BP3C3 BP3RC3 BP3C4 BP3RC4

MATERIAL	DWN D.F.C. 1-25-74	PRIME COMPUTER, INC. MATICK, MASS.	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES. –DIMENSIONS ARE IN INCHES –TOLERANCES .XX ±.03 .XXX ±.005 ANGLES ±1/2°	CHK	VERSATEC BP2 I/O REGISTER	
	ENG.		
	APPRD		
	USED ON 3009-901 NEXT ASSY	SCALE SHEET 30A OF	SIZE C DWG. NO. LBD 1528 A

III-32A

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74157 16M

[13] DAT01+
B20D09+
DAT02+
B20D10+
DAT03+
B20D11+
DAT04+
B20D12+
[31] B2ENL8-

1A 1B 2A 2B 3A 3B 4A 4B S G
1Y 2Y 3Y 4Y

GB2D01+
GB2D02+
GB2D03+
GB2D04+

74175 16N

1D 2D 3D 4D T C

BP2D01+ BP2D01-
BP2D02+ BP2D02-
BP2D03+ BP2D03-
BP2D04+ BP2D04-

74157 18M

DAT05+
B20D13+
DAT06+
B20D14+
DAT07+
B20D15+
DAT08+
B20D16+
[31] B2ENL8-

GB2D05+
GB2D06+
GB2D07+
GB2D08+

74175 18N

BP2D05+ BP2D05-
BP2D06+ BP2D06-
BP2D07+ BP2D07-
BP2D08+ BP2D08-

74157 20M

DAT09+
B20D01+
DAT10+
B20D02+
DAT11+
B20D03+
DAT12+
B20D04+
GND

GB2D09+
GB2D10+
GB2D11+
GB2D12+

74175 20N

BP2D09+ BP2D09-
BP2D10+ BP2D10-
BP2D11+ BP2D11-
BP2D12+ BP2D12-

74157 22M

DAT13+
B20D05+
DAT14+
B20D06+
DAT15+
B20D07+
DAT16+
B20D08+
GND

GB2D13+
GB2D14+
GB2D15+
GB2D16+

74175 22N

BP2D13+ BP2D13-
BP2D14+ BP2D14-
BP2D15+ BP2D15-
BP2D16+ BP2D16-

[31] TBF2R-

74H01 18P

B20D05+ B20D06+ B20D07+ B20D08+
FB20ML+

74H08 22P

B20D13+ B20D14+ B20D15+ B20D16+
FB20MR+

+5 14P

CE-1 B20D01+
CE-3 B20D02+
CE-5 B20D03+
CE-7 B20D04+

+5 14P

CE-7 B20D05+
CE-11 B20D06+
CE-13 B20D07+
CE-15 B20D08+
FND03
FND02
FND01
FND00

+5 14P

CE-17 B20D09+
CE-19 B20D10+
CE-21 B20D11+
CE-23 B20D12+
GOULD
STDBY
VCNFLT
PAPER LOW

+5 14P 12P

CE-25 B20D13+
CE-27 B20D14+
CE-29 B20D15+
CE-31 B20D16+

9602 6G

SHL
BP3C3
BP3RC3
PLUPB2
Q BP2STRB+

9602 6G

B2TR-
PLUPB
BP3C4
BP3RC4
PLUPB2
Q 9 B2ENDEV-

RC 107

5.1K 10K 4G
BP3C3 BP3RC3 BP3C4 BP3RC4

7408 41H

CBP2DR-
SYSCLK
B2RRSY-

7400 22K

[31] BP20TMD+
SB2IO+

7400 18K 7404 22L

B2ENDEV-
[31] B2TRDY-
B2EDEV+
B2EDEV-

74H04 14K

31 BP2INMD+
FB20ML+

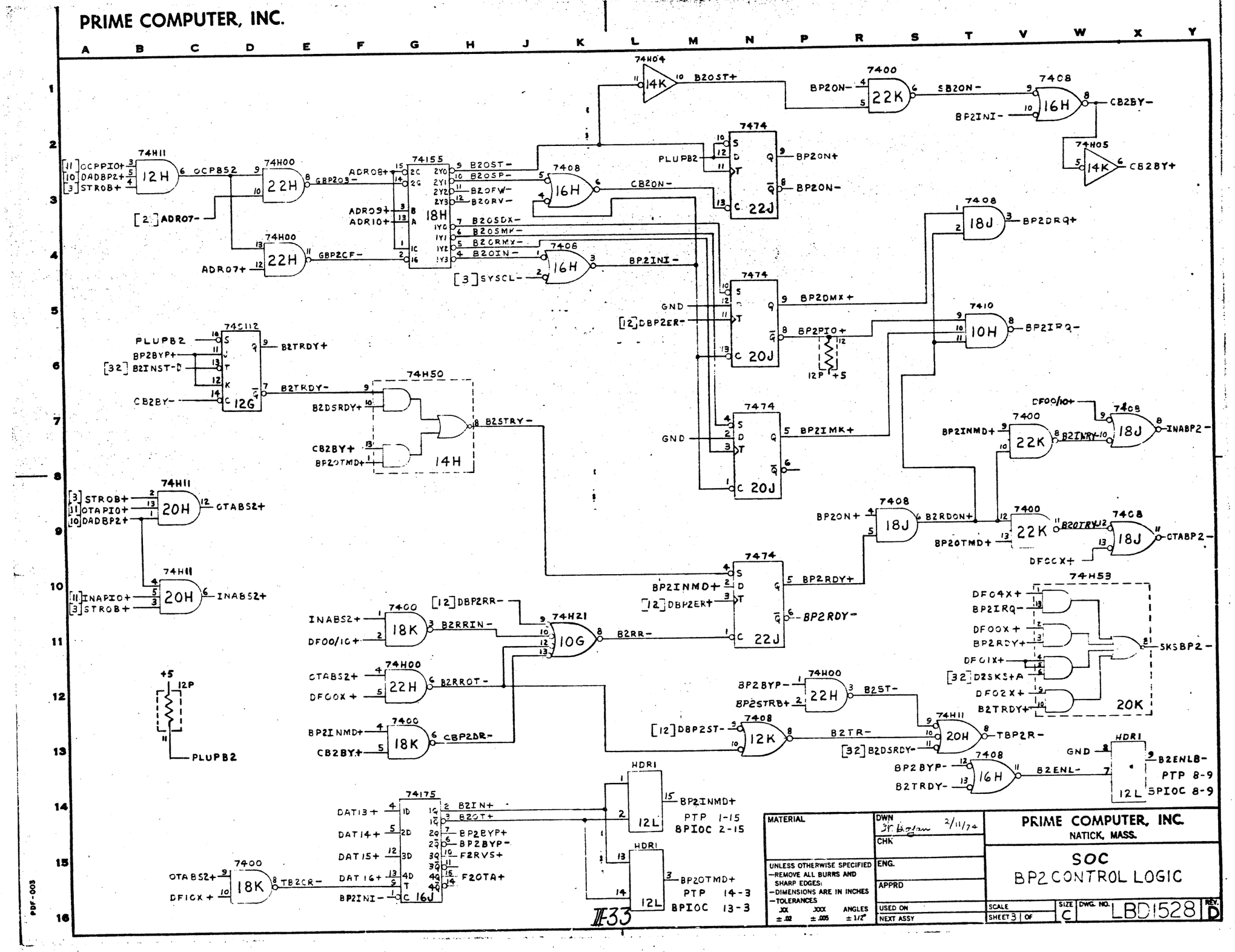
7400 14J

BP2BYP-
FB20MR+

III-32B

MATERIAL	DWN Paul Beatrice 7-28-75	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	GOULD BP2 I/O REGISTER	
	ENG Dick Lupo 8/6/75		
	APPRD		
	USED ON 3008-901 NEXT ASSY	SCALE — SHEET 30 OF	SIZE C DWG. NO. LBD1528 REV. A

PSP-005



MATERIAL	DWN JR Bogan 2/11/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	SOC BP2 CONTROL LOGIC
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF
		SIZE C DWG. NO. LBD1528 REV. D

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74H04 14K BZOST+

7400 22K BP2ON- SB2ON-

7408 16H BP2INI- CB2BY-

74H05 14K CB2BY+

7474 PLUPB2 BP2ON+ BP2ON- 22J

74H11 12H OCPB52 OCPPIO+ DADBP2+ STROB+

74H00 22H GBP2CF- ADR07+ [2] ADR07-

74H00 22H GBP2D3- ADR08+

74155 18H ADR09+ ADR10+ BZOST- BZOSP- BZOFW- BZORV- BZOSDX- BZOSMP- BZORMX- BZOIN-

7408 16H CB2ON- BP2INI- [3] SYSCL-

7408 18J BP2DRQ+

7474 GND [12] DBP2ER- BP2DMK+ BP2PIO+ 20J 12P +5

7410 10H BP2IRQ-

74S112 PLUPB2 BP2BYP+ [32] BZINST-0 CE2BY- BZTRDY+ BZTRDY- 12G

74H50 BZDSRDY+ CB2BY+ BP2[illegible]MD+ BZSTRY- 14H

7474 GND BP2IMK+ 20J

7400 BP2INMD+ 22K B2TMRY-10

7408 18J ZNABP2-

DF00/10+

74H11 [3] STROB+ [11] OTAPIO+ [10] DADBP2+ 20H OTABS2+

74H11 [11] INAPIO+ [3] STROB+ 20H INABS2+

7474 BP2INMD+ [12] DBP2ER+ BP2RDY+ BP2RDY- 22J

7400 BP2ON+ 18J B2RDON+

7400 BP2OTMD+ 22K B2OTRY-12

7408 18J OTABP2-

DF0CX+

74H55 DF04X+ BP2IRQ- DF00X+ BP2RDY+ DF01X+ [38] D2SKS+A DF02X+ B2TRDY+ 20K SKSBP2-

INABS2+ DF00/10+ 7400 18K B2RRIN- 74H21 10G B2RR-

OTABS2+ DF0CX+ 74H00 22H B2RROT-

BP2INMD+ CB2BY+ 7400 18K CBP2DR-

BP2BYP- BP2STRB+ 74H00 22H B2ST-

[12] DBP2ST- 7408 12K B2TR-

[38] B2DSRDY- 74H11 20H TBP2R-

BP2BYP- B2TRDY- 7408 16H B2ENL-

GND W112 B2ENLB- PTP 8-9 BPIOC 8-9 12L

+5 12P PLUPB2

74175 DAT13+ DAT14+ DAT15+ DAT16+ B2IN+ BP2BYP+ BP2BYP- F2PVS+ F2OTA+ 16J

OTABS2+ DF0CX+ 7400 18K TB2DR-

W112 BP2INMD+ PTP 1-15 BPIOC 2-15 12L

W112 BP2OTMD+ PTP 14-3 BPIOC 13-3 12L

IIF33-A

MATERIAL	DWN JF Wagman 2/11/74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	VERSATEC BP2 CONTROL LOGIC	
	ENG.		
	APPRD		
	USED ON 3009-901 NEXT ASSY	SCALE SHEET 1 OF	SIZE C DWG. NO. LBD1528 REV A

PSF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74H04 14K B20ST+

BP20N- 7400 22K SB20N- 7408 16H CB2BY-

BP2INI-

74H05 14K CB2BY+

74H11 12H GCPBS2 GCPPIO+ DADBP2+ STROB+

74H00 22H GBP2CB- ADR07+

74H00 22H GBP2CF- ADR07+

74155 ADR08+ ADR09+ ADR10+ 18H B20ST- B20SP- B20FW- B20RV- B20SDX- B20SMK- B20RMX- B20IN-

7408 16H CB2ON- BP2INI-

[3] SYSCL-

7474 PLUPB2 BP20N+ BP20N- 22J

7408 18J BP2DRQ+

7474 GND [12] DBP2ER- BP2DMK+ BP2PIO+ 20J

7410 10H BP2IRQ-

12P +5

74S112 PLUPB2 BP2BYP+ [32] B2INST- CB2BY- 12G B2TRDY+ B2TRDY-

74H50 B2DSRDY+ CB2BY+ BP2DTMD+ 14H B2STRY-

7474 GND BP2IMK+ 20J

DF00/10+ 7400 BP2INMD+ 22K B2INRY-10 7408 18J INABP2-

74H11 [3] STROB+ [11] OTAPIO+ [10] DADBP2+ 20H OTABS2+

74H11 [11] INAPIO+ [3] STROB+ 20H INABS2+

7408 18J BP2RDON+ BP20N+

7400 22K B2OTRY-12 BP20TMD+ DF00X+ 7408 18J OTABP2-

7474 BP2INMD+ [2] DBP2ER+ BP2RDY+ BP2RDY- 22J

74H53 DF04X+ BP2IRQ- DF00X+ BP2RDY+ DF01X+ [38] D2SKS+A DF02X+ B2TRDY+ 20K SKSBP2-

+5 12P PLUPB2

7400 INABS2+ DF00/10+ 18K B2RRIN- 74H21 10G B2RR-

74H00 OTABS2+ DF00X+ 22H B2RRQT-

7400 BP2INMD+ CB2BY+ 18K CBP2DR-

74H00 BP2BYP- BP2STRB+ 22H B2ST-

7408 [12] DBP2ST- 12K B2TR-

74H11 20H TBP2R-

[32] B2DSRDY-

7408 BP2BYP- B2TRDY- 16H B2ENL-

W138 GND B2ENLB- PTP 8-9 BPIOC 8-9 12L

74175 DAT13+ DAT14+ DAT15+ DAT16+ BP2INI- 16J B2IN+ B2OT+ BP2BYP+ BP2BYP- F2RVS+ F2CTA+

7400 OTABS2+ DF10X+ 18K TB2CR-

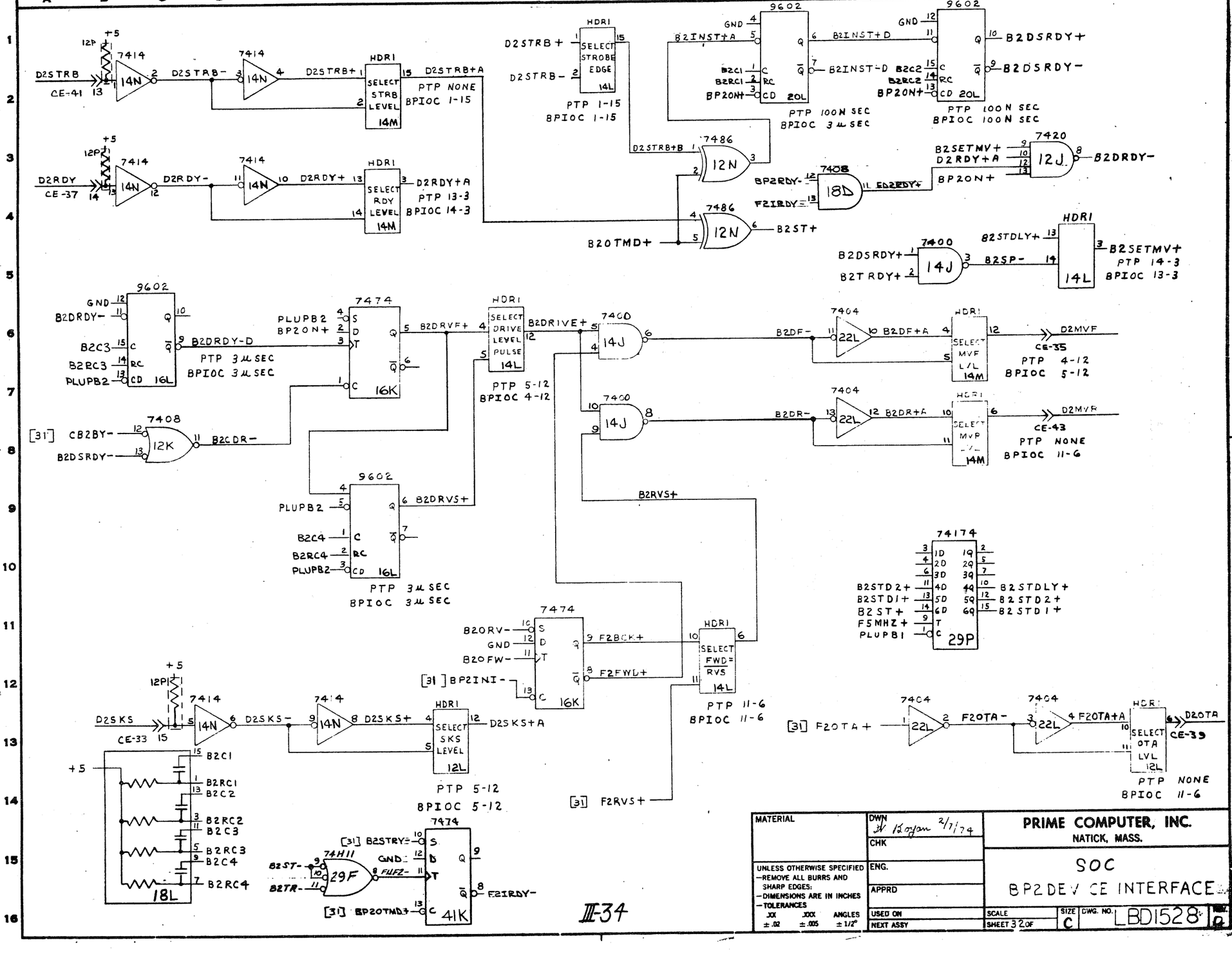
W138 BP2INMD+ PTP 1-15 BPIOC 2-15 12L

BP2OTMD+ PTP 14-3 BPIOC 13-3 12L

II-33B

MATERIAL	DWN JH Hogan 2/11/74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	GOULD BP2 CONTROL LOGIC	
	ENG. 8/8/75		
	APPRD		
	USED ON 3009-901 NEXT ASSY	SCALE	SIZE C DWG. NO. LBD1528 REV. A
		SHEET 5 OF	

PDF-003



MATERIAL	DWN H Boyan 2/7/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ± 1/2°	ENG.	SOC BP2 DEV CE INTERFACE	
	APPRD		
	USED ON	SCALE	SIZE C
	NEXT ASSY	SHEET 32 OF	DWG. NO. LBD1528 REV. C

PBF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

D2MVF
D2STRB
CE-41
7414 14N
D2STRB-
7414 14N
D2STRB+
W107 SELECT STRB LEVEL 14M
D2STRB+A
PTP NONE
BPIOC 1-15

D2STRB+
D2STRB-
W132 SELECT STROBE EDGE 14L
PTP 1-15
BPIOC 1-15

B2INST+A
9602 GND B2C1 B2RC1 BP20N+ CD 20L
B2INST+D
B2INST-D
9602 GND B2C2 B2RC2 BP20N+ CD 20L
PTP 100N SEC
BPIOC 3 μ SEC
PTP 100N SEC
BPIOC 100N SEC
B2DSRDY+
B2DSRDY-

D2RDY
CE-37
7414 14N
D2RDY-
7414 14N
D2RDY+
W107 SELECT RDY LEVEL 14M
D2RDY+A
PTP 13-3
BPIOC 14-3

D2STRB+B
7486 12N
B20TMD+
7486 12N
B2ST+

BP2RDY-
F2IRDY-
7408 18D
ED2RDY+
B2SETMV+
D2RDY+A
BP20N+
7420 12J
B2DRDY-

B2DSRDY+
B2TRDY+
7400 14J
B2STDLY+
B2SP-
W132 14L
B2SETMV+
PTP 14-3
BPIOC 13-3

GND B2DRDY- B2C3 B2RC3 PLUPB2
9602 CD 16L
B2DRDY-D
PTP 3 μ SEC
BPIOC 3 μ SEC

PLUPB2
BP20N+
7474 16K
B2DRVE+
W132 SELECT DRIVE LEVEL PULSE 14L
PTP 5-12
BPIOC 4-12

[3T] CB2BY-
B2DSRDY-
7408 12K
B2CDR-

7400 14J
B2DF-
7404 22L
B2DF+A
W107 SELECT MVF L/L 14M
D2MVF
CE-35
PTP 4-12
BPIOC 5-12

7400 14J
B2DR-
7404 22L
B2DR+A
W107 SELECT MVR L/L 14M
D2MVR
CE-43
PTP NONE
BPIOC 11-6

B2RVS+

PLUPB2
B2C4 B2RC4 PLUPB2
9602 CD 16L
B2DRVS+
PTP 3 μ SEC
BPIOC 3 μ SEC

74174
B2STD2+
B2STD1+
B2ST+
F5MHZ+
PLUPB1
29P
B2STDLY+
B2STD2+
B2STD1+

B2ORV-
GND
B2OFW-
[3] BP2INI-
7474 16K
F2BCK+
F2FWD+
W132 SELECT FWD=/RVS 14L
PTP 11-6
BPIOC 11-6

READY
D2SKS
CE-38
7414 14N
D2SKS-
7414 14N
D2SKS+
W112 SELECT SKS LEVEL 12L
D2SKS+A
PTP 5-12
BPIOC 5-12

+5
R21
B2RC1
B2RC2
B2RC3
B2RC4
18L

[3] F2RVS+

[3] F2OTA+
7404 22L
F2OTA-
7404 22L
F2OTA+A
W112 SELECT OTA LVL 12L
SPP
D2OTA
CE-39
PTP NONE
BPIOC 11-6

[3] B2STRY-
B2ST-
B2TR-
74H11 29F
GND
F1IF2-
[3] BP20TMD+
F2IRDY-

II-34-A

MATERIAL	DWN J. Boyan 2/7/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES — DIMENSIONS ARE IN INCHES — TOLERANCES	ENG.	VERSATEC
	APPRD	BP2 DEVICE INTERFACE
	USED ON 3089-901 / NEXT ASSY	SCALE — SIZE C — LBD152

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

(D2MVF) D2STRB
CE-41 13
+5 12P
7414 14N
D2STRB-
D2STRB+
W136 SELECT STRB LEVEL 14M
D2STRB+A
PTP NONE
BPIOC 1-15

D2STRB+ 1
D2STRB- 2
W10 SELECT STROBE EDGE 14L
PTP 1-15
BPIOC 1-15

9602
GND 4
B2INST+A 5
B2C1 1
B2RC1 2
BP20N+ 3
C RC CD 20L
Q 6 B2INST+D
Q 7 B2INST-D
PTP 100N SEC
BPIOC 3 μ SEC

9602
GND 12
B2C2 15
B2RC2 14
BP20N+ 13
C RC CD 20L
Q 10 B2DSRDY+
Q 9 B2DSRDY-
PTP 100N SEC
BPIOC 100N SEC

(SINTP) D2RDY
CE-37 14
+5 12P
7414 14N
D2RDY-
D2RDY+
W136 SELECT RDY LEVEL 14M
D2RDY+A
PTP 13-3
BPIOC 14-3

D2STRB+B 1
7486 12N
B20TMD+
7486 12N
B2ST+

BP2RDY- 12
F2IRDY- 13
7408 18D
ED2RDY+

B2SETMV+ 9
D2RDY+A 10
BP20N+ 12
13
7420 12J
B2DRDY-

B2DSRDY+ 1
B2TRDY+ 2
7400 14J
B2SP- 14
W10 B2STDLY+ 13
14L
B2SETMV+
PTP 14-3
BPIOC 13-3

9602
GND 12
B2DRDY- 11
B2C3 15
B2RC3 14
PLUPB2 13
C RC CD 16L
Q 10
Q 9 B2DRDY-D
PTP 3 μ SEC
BPIOC 3 μ SEC

PLUPB2 4
BP20N+ 2
3
7474 S D T C 16K
Q 5 B2DRVF+
Q 6
1

W10 SELECT DRIVE LEVEL PULSE 14L
B2DRIVE+ 5
PTP 5-12
BPIOC 4-12

7400 14J
7400 14J
B2RV5+

B2DF- 11
7404 22L
B2DF+A 10
W136 SELECT M/F L/L 14M 12
D2MVF
CE-35
PTP 4-12
BPIOC 5-12
(D2STRB)

B2DR- 13
7404 22L
B2DR+A 12
W136 SELECT M/F L/L 14M 6
D2MVR
CE-43
PTP NONE
BPIOC 11-6
FNSTRB

[31] CB2BY- 12
B2DSRDY- 13
7408 12K
B2CDR-

9602
PLUPB2 5
B2C4 1
B2RC4 2
PLUPB2 3
C RC CD 16L
Q 4
Q 7 B2DRVS+
PTP 3 μ SEC
BPIOC 3 μ SEC

74174
3 1D 1Q 2
4 2D 2Q 5
6 3D 3Q 7
11 4D 4Q 10 B2STDLY+
13 5D 5Q 12 B2STD2+
14 6D 6Q 15 B2STD1+
9 T
1 C 29P
B2STD2+
B2STD1+
B2ST+
F5MHZ+
PLUPB1

7474
B20RV- 10
GND 12
B20FW- 11
[31] BP2INI- 13
S D T C 16K
Q 9 F2BCK+
Q 5 F2FWD+
W10 SELECT FWD REV 14L
10 6
11
PTP 11-6
BPIOC 11-6

[31] F2RVS+

SELECT D2SKS
CE-33 15
+5 12P
7414 14N
D2SKS-
9 14N 8 D2SKS+
W138 SELECT SKS LEVEL 12L
12 D2SKS+A
PTP 5-12
BPIOC 5-12

RC117 18L
+5
15 B2C1
1 B2RC1
13 B2C2
3 B2RC2
11 B2C3
5 B2RC3
9 B2C4
7 B2RC4

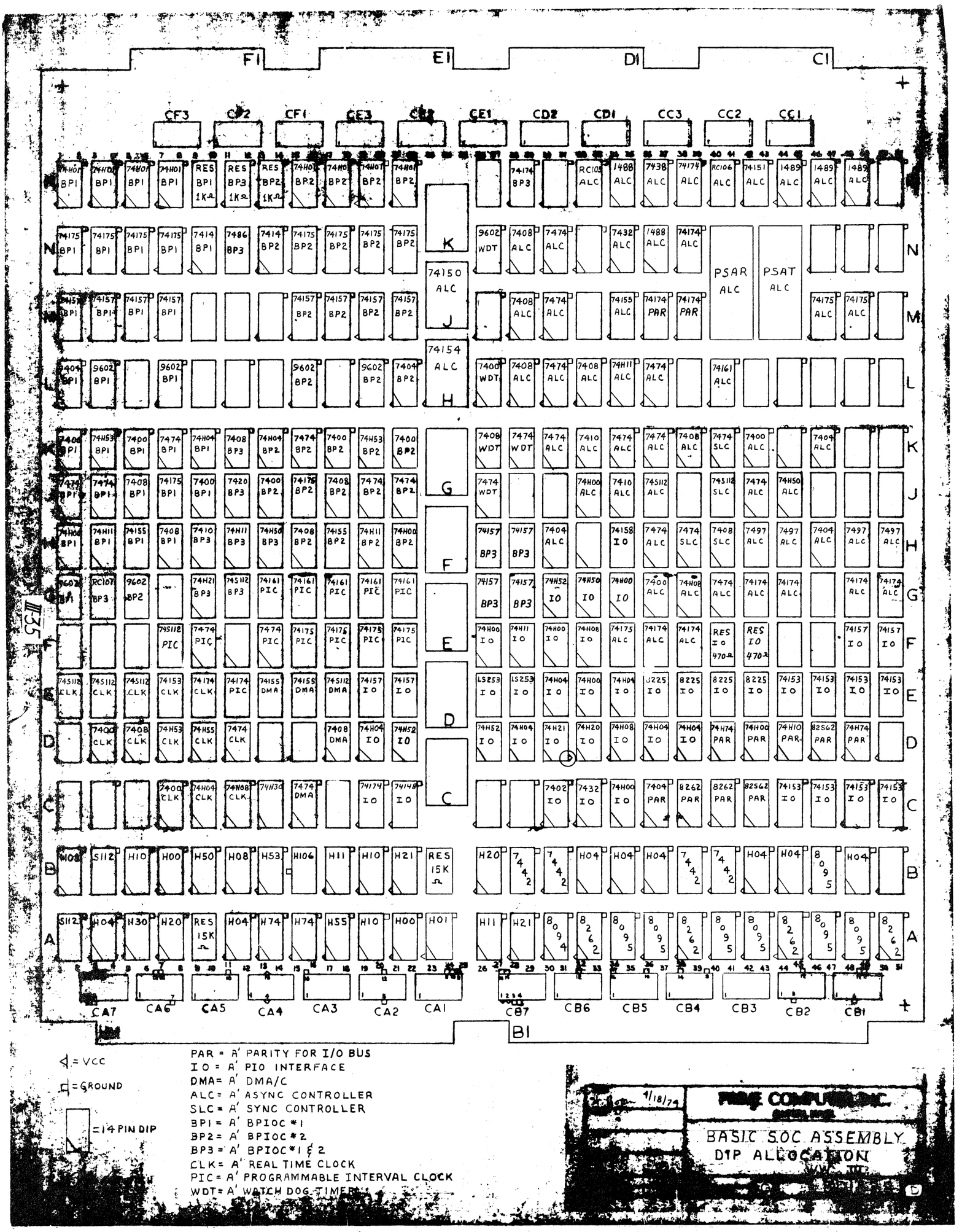
[31] B2STRV- 10
74H11 29F
GND 12
B2ST- 9
B2TR- 11
8 F2IRD-
S D T C 41K
Q 9
Q 8 F2IRDY-
[31] BP20TMD+ 13
7474

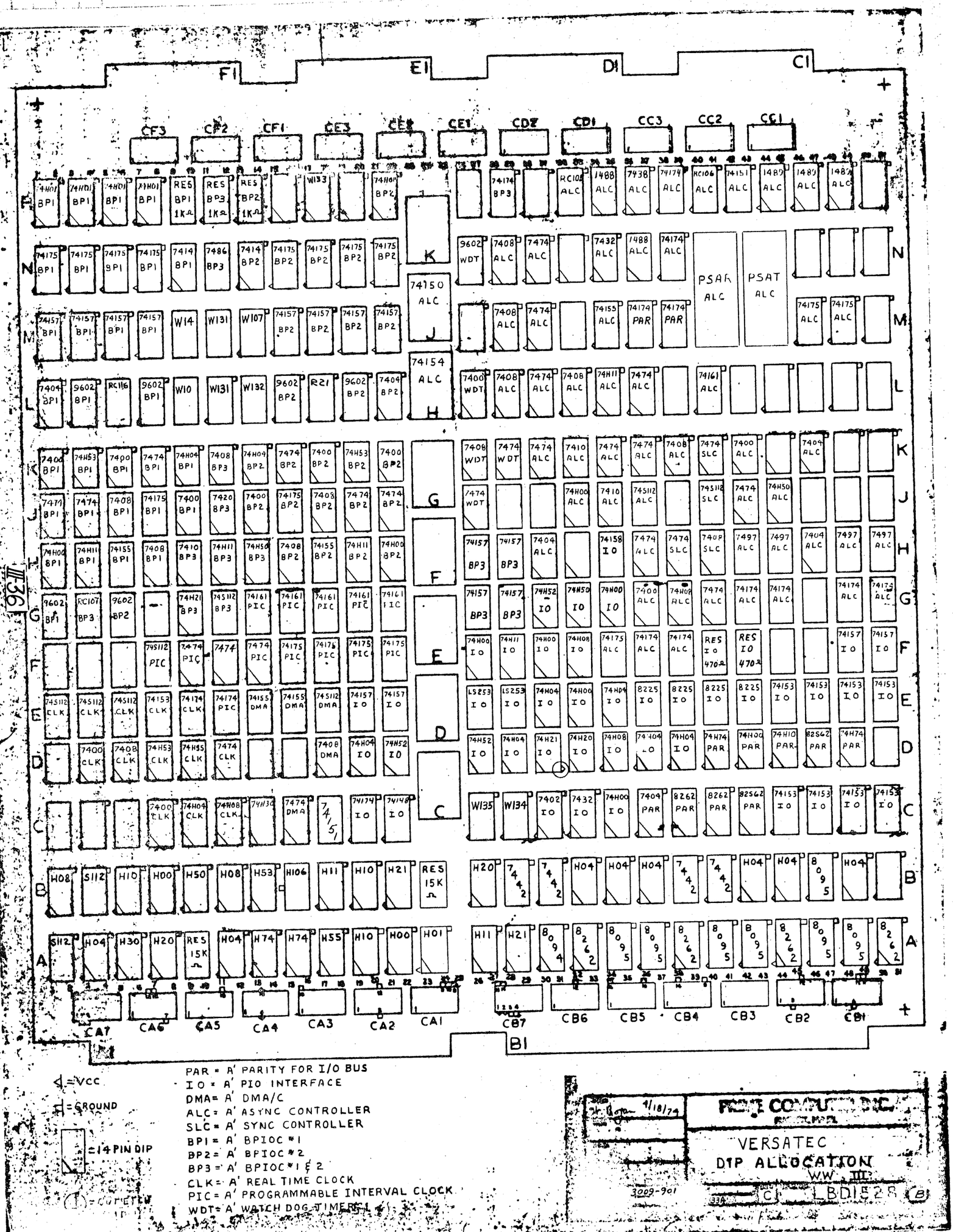
[31] F20TA+
7404 22L
F20TA-
7404 22L
4 F20TA+A
W138 SELECT DTA LVL 12L
RESET D20TA
CE-39
PTP NONE
BPIOC 11-6

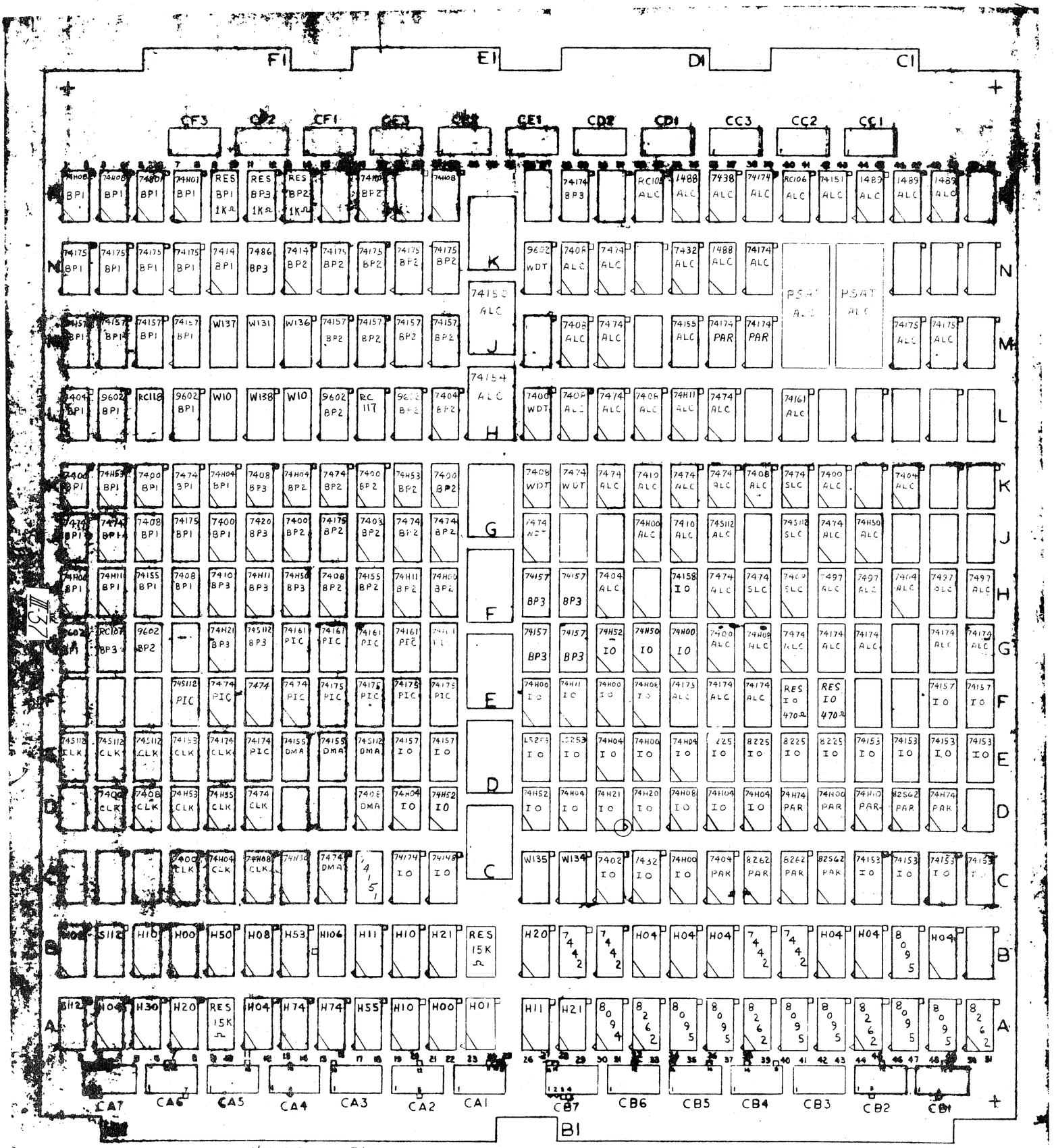
MATERIAL	DWN 7-28-75 Paula Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	GOULD BP2 DEVICE INTERFACE	
	ENG Nick Lupo 8/6/75		
	APPRD		
USED ON	NEXT ASSY	SCALE	SIZE C DWG NO LBD1528 REV B
		SHEET 32 BOF	

III-34B

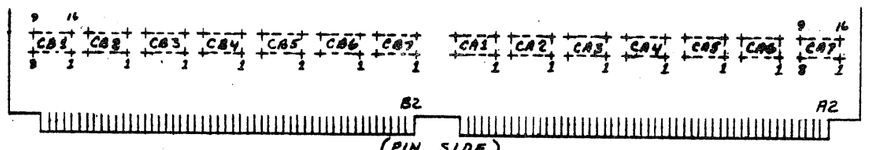
PSF-005


F1
E1
D1
C1
CF3
CF2
CF1
CE3
CE2
CE1
CD2
CD1
CC3
CC2
CC1
PSAR ALC
PSAT ALC
74150 ALC
74154 ALC
CA7
CA6
CA5
CA4
CA3
CA2
CA1
CB7
CB6
CB5
CB4
CB3
CB2
CB1
B1
= VCC
= GROUND
= 14 PIN DIP
PAR = A' PARITY FOR I/O BUS
IO = A' PIO INTERFACE
DMA = A' DMA/C
ALC = A' ASYNC CONTROLLER
SLC = A' SYNC CONTROLLER
BPI = A' BPIOC #1
BP2 = A' BPIOC #2
BP3 = A' BPIOC #1 & 2
CLK = A' REAL TIME CLOCK
PIC = A' PROGRAMMABLE INTERVAL CLOCK
WDT = A' WATCH DOG TIMER
1/18/74
PRIME COMPUTER, INC.
BASIC SOC ASSEMBLY
DIP ALLOCATION
D


F1
E1
D1
C1
CF3
CF2
CF1
CE3
CE2
CE1
CD2
CD1
CC3
CC2
CC1
PSAR ALC
PSAT ALC
74150 ALC
74154 ALC
CA7
CA6
CA5
CA4
CA3
CA2
CA1
CB7
CB6
CB5
CB4
CB3
CB2
CB1
B1
PAR = A' PARITY FOR I/O BUS
IO = A' PIO INTERFACE
DMA = A' DMA/C
ALC = A' ASYNC CONTROLLER
SLC = A' SYNC CONTROLLER
BPI = A' BPIOC #1
BP2 = A' BPIOC #2
BP3 = A' BPIOC #1 & 2
CLK = A' REAL TIME CLOCK
PIC = A' PROGRAMMABLE INTERVAL CLOCK
WDT = A' WATCH DOG TIMER
= VCC
= GROUND
= 14 PIN DIP
VERSATEC
DIP ALLOCATION
3009-901
LBD1528


F1
E1
D1
C1
CF3
CF2
CF1
CE3
CE2
CE1
CD2
CD1
CC3
CC2
CC1
CA7
CA6
CA5
CA4
CA3
CA2
CA1
CB7
CB6
CB5
CB4
CB3
CB2
CB1
A1
B1
PAR = A' PARITY FOR I/O BUS
IO = A' PIO INTERFACE
DMA = A' DMA/C
ALC = A' ASYNC CONTROLLER
SLC = A' SYNC CONTROLLER
BPI = A' BPIOC #1
BP2 = A' BPIOC #2
BP3 = A' BPIOC #1 & 2
CLK = A' REAL TIME CLOCK
PIC = A' PROGRAMMABLE INTERVAL CLOCK
WDT = A' WATCH DOG TIMER
= VCC
= GROUND
= 14 PIN DIP
7-28-75
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
GOULD
DIP ALLOCATION
WW II
5008-301
NONE
C
LBD 1528

LTR	DATE	REVISION	DR.	CK.



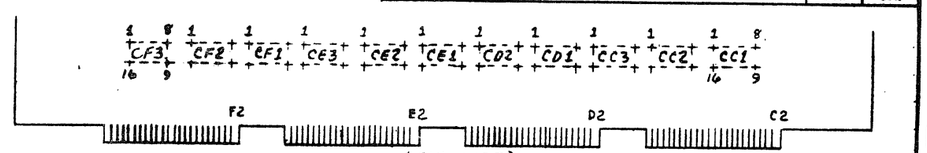
(PIN SIDE)

NAME	DIP SITE	CONN PIN
VCC1	CA7-15,16	CA-1
VCC1	CA7-15,16	CA-2
SHIELD(GND)	CA7-3	CA-3
BPCDCPN+	CA7-1	CA-4
BPCDEN +	CA7-8	CA-5
GND	CA7-2,4,14,13	CA-6
BPCDPNO -	CA7-12	CA-7
BPCDPNA -	CA7-4	CA-8
BPCDPNB -	CA7-10	CA-9
BPCDPNC -	CA7-5	CA-10
BPCDPND -	CA6-16	CA-11
BPCDPNE -	CA7-7	CA-12
BPCDPNF -	CA6-14	CA-13
BPCDPNG -	CA7-11	CA-14
BPCDPNH -	CA6-2	CA-15
BPCIEN +	CA7-9	CA-16
BPCIPND -	CA6-4	CA-17
BPCIPNA -	CA6-15	CA-18
BPCIPNB -	CA6-6	CA-19
BPCIPNC -	CA6-3	CA-20
BPCIPND -	CA6-8	CA-21
SHIELD(GND)	CA6-5	CA-22
BPCICPN +	CA6-11	CA-23
GND	CA6-1,12,13	CA-24
BPCCNI +	CA6-9	CA-25
SHIELD(GND)	CA6-10	CA-26
	CA5-15	CA-27
	CA5-16	CA-28
	CA5-13	CA-29
BPCEOR +	CA5-14	CA-30
	CA5-2	CA-31
	CA5-1	CA-32
	CA5-4	CA-33
	CA5-3	CA-34
	CA5-6	CA-35
	CA5-5	CA-36
	CA5-8	CA-37
BPCIOVI -	CA5-7	CA-38
	CA5-11	CA-39
	CA5-12	CA-40
	CA5-9	CA-41
GND	CA5-10	CA-42
BMCWDLR+	CA4-15	CA-43
	CA4-16	CA-44
	CA4-14	CA-45
	CA4-1	CA-46
BMCWDLL +	CA4-2	CA-47
SHIELD(GND)	CA4-3	CA-48
VCC1	CA4-4,13	CA-49
VCC1	CA4-4,13	CA-50

NAME	DIP SITE	CONN PIN
BMCABL +	CA4-6	CA-51
	CA4-5	CA-52
	CA4-8	CA-53
	CA4-7	CA-54
	CA4-11	CA-55
BMAPEL+	CA4-12	CA-56
BMAPER+	CA4-9	CA-57
BMDPEL-	CA4-10	CA-58
BMDPER-	CA3-15	CA-59
GND	CA3-16	CA-60
BMD01 +	CA3-13	CA-61
BMD02 +	CA3-1	CA-62
BMD03 +	CA3-2	CA-63
BMD04 +	CA3-3	CA-64
BMD05 +	CA3-4	CA-65
BMD06 +	CA3-5	CA-66
BMD07 +	CA3-6	CA-67
BMD08 +	CA3-7	CA-68
BMD09 +	CA3-8	CA-69
BMD10 +	CA3-12	CA-70
BMD11 +	CA3-11	CA-71
BMD12 +	CA3-10	CA-72
BMD13 +	CA3-9	CA-73
BMD14 +	CA2-16	CA-74
BMD15 +	CA2-15	CA-75
BMD16 +	CA2-1	CA-76
BMDLP-	CA2-13	CA-77
BMDRP-	CA2-3	CA-78
BMCSELC-	CA2-2	CA-79
GND	CA2-5,12	CA-80
BMCSELB-	CA2-4	CA-81
BMCSELV-	CA2-7	CA-82
BMCDINH-	CA2-6	CA-83
BMCWRB -	CA2-10	CA-84
BMCWLB -	CA2-8	CA-85
BMCRFSH-	CA1-16	CA-86
BMCEXS1-	CA2-11	CA-87
BMCWSTRB-	CA1-14	CA-88
BMCEXS2-	CA2-9	CA-89
BPCFCLK +	CA1-1	CA-90
BMCSS01-	CA1-15	CA-91
BPCIRQ -	CA1-3	CA-92
BMCSS02-	CA1-13	CA-93
BPCDRQ -	CA1-6	CA-94
BMCSS03-	CA1-2	CA-95
BMCPRCH-	CA1-7	CA-96
BMCCNBL-	CA1-4	CA-97
GND	CA1-3,10,11	CA-98
VCC2	CA2-8	CA-99
VCC2	SPARE	CA-100

NAME	DIP SITE	CONN PIN
VCC1	CB7-1,2	CB-1
VCC1	CB7-1,2	CB-2
GND	CB7-3,4,5,6	CB-3
ISOSPARE	CB7-5	CB-4
BMA99 -	CB7-8	CB-5
BMA00 -	CB7-7	CB-6
BMA01 -	CB7-12	CB-7
BMA02 -	CB7-13	CB-8
BMA03 -	CB7-10	CB-9
BMA04 -	CB7-11	CB-10
BMA05 -	CB6-16	CB-11
BMA06 -	CB7-9	CB-12
BMA07 -	CB6-14	CB-13
BMA08 -	CB6-15	CB-14
BMA09 -	CB6-2	CB-15
BMA10 -	CB6-1	CB-16
BMA11 -	CB6-4	CB-17
BMA12 -	CB6-3	CB-18
BMA13 -	CB6-6	CB-19
BMA14 -	CB6-5	CB-20
BMA15 -	CB6-8	CB-21
BMA16 -	CB6-7	CB-22
BMA.P -	CB6-11	CB-23
BMARP -	CB6-13	CB-24
HPWRFL -	CB6-9	CB-25
GND	CB6-12	CB-26
VCORE1	CB5-15	CB-27
VCORE1	CB6-10	CB-28
BPA01 +	CB5-13	CB-29
GND	CB5-16	CB-30
BPA02 +	CB5-2	CB-31
BPA03 +	CB5-1	CB-32
BPA04 +	CB5-4	CB-33
BPA05 +	CB5-3	CB-34
BPA06 +	CB5-6	CB-35
BPA07 +	CB5-5	CB-36
BPA08 +	CB5-8	CB-37
BPA09 +	CB5-7	CB-38
BPAIO +	CB5-11	CB-39
BPA11 +	CB5-14	CB-40
HSYSCLR -	CB5-9	CB-41
GND	CB5-10	CB-42
VCORE2	CB4-15	CB-43
VCORE2	CB4-16	CB-44
BPDPEL -	CB4-13	CB-45
GND	CB4-1,14	CB-46
BPDPER -	CB4-2	CB-47
BPAPEL -	CB4-3	CB-48
BPA99 +	CB4-4	CB-49
BPA00 +	CB4-5	CB-50

NAME	DIP SITE	CONN PIN
BPA12 +	CB4-6	CB-51
BPA13 +	CB4-7	CB-52
BPA14 +	CB4-8	CB-53
BPA15 +	CB4-12	CB-54
BPA16 +	CB4-11	CB-55
BPA1P +	CB4-10	CB-56
GND	CB4-9	CB-57
BPARP +	CB3-16	CB-58
BPCPIO +	CB3-15	CB-59
BPAPER -	CB3-14	CB-60
BPC60CY +	CB3-13	CB-61
BPCREDY -	CB3-1	CB-62
BPDLP +	CB3-2	CB-63
	CB3-3	CB-64
BPD01 +	CB3-4	CB-65
BPDRP +	CB3-5	CB-66
BPD02 +	CB3-6	CB-67
BPD03 +	CB3-7	CB-68
BPD04 +	CB3-8	CB-69
BPD05 +	CB3-12	CB-70
BPD06 +	CB3-11	CB-71
BPD07 +	CB3-10	CB-72
BPD08 +	CB3-9	CB-73
BPD09 +	CB2-16	CB-74
BPD10 +	CB2-15	CB-75
BPD11 +	CB2-14	CB-76
VI2 -	CB2-13	CB-77
VI2 -	CB2-1	CB-78
BPD12 +	CB2-2	CB-79
GND	CB2-3,12	CB-80
BPD13 +	CB2-4	CB-81
BPD14 +	CB2-5	CB-82
BPD15 +	CB2-6	CB-83
BPD16 +	CB2-7	CB-84
BPCMOD0 +	CB2-8	CB-85
BPCMOD1 +	CB2-10	CB-86
BPCMOD2 +	CB2-11	CB-87
BPCMOD3 +	CB1-16	CB-88
BPCINMD +	CB2-9	CB-89
BPCSCLK +	CB1-14	CB-90
VI2 +	CB1-15	CB-91
VI2 +	NOT USED	CB-92
HRUN -	CB1-13	CB-93
HRUN -	CB1-3	CB-94
BPCSTRB +	CB1-2	CB-95
GND	CB1-4,14,12	CB-96
VSS	CB1-5	CB-97
VSS	NOT USED	CB-98
VBB	CB1-6	CB-99
VBB	NOT USED	CB-100



(PIN SIDE)

NAME	DIP SITE	CONN PIN
EIAC4+	CC1-8	CC-1
GND	CC1-7	CC-2
EIAC3+	CC1-6	CC-3
GND	CC1-5	CC-4
EIAC3+	CC1-9	CC-5
GND	CC1-10	CC-6
EIAC2+	CC1-11	CC-7
GND	CC1-12	CC-8
EIAC1+	CC1-13	CC-9
GND	CC1-14	CC-10
TXEIA3-	CC1-15	CC-11
GND	CC1-16	CC-12
TXEIA4-	CC1-4	CC-13
GND	CC1-3	CC-14
TXEIA1-	CC1-2	CC-15
GND	CC1-1	CC-16
TXEIA2-	CC2-8	CC-17
GND	CC2-7	CC-18
EIAC1+	CC2-6	CC-19
GND	CC2-5	CC-20
INBIT3-	CC2-9	CC-21
GND	CC2-10	CC-22
INBIT4-	CC2-11	CC-23
GND	CC2-12	CC-24
INBIT3-	CC2-13	CC-25
GND	CC2-14	CC-26
INBIT2-	CC2-15	CC-27
GND	CC2-16	CC-28
INBIT1-	CC2-4	CC-29
GND	CC2-3	CC-30
INBIT1-	CC2-2	CC-31
GND	CC2-1	CC-32
RXEIA1+	CC3-8	CC-33
GND	CC3-7	CC-34
RXEIA2+	CC3-6	CC-35
GND	CC3-5	CC-36
PREXCLK+	CC3-9	CC-37
GND	CC3-10	CC-38
RXEIA3+	CC3-11	CC-39
GND	CC3-12	CC-40
RXEIA4+	CC3-13	CC-41
GND	CC3-14	CC-42
PTEXCLK+	CC3-15	CC-43
GND	CC3-16	CC-44

NAME	DIP SITE	CONN PIN
RXEIA1+	CC3-4	CD-1
GND	CC3-3	CD-2
CLIN+	CC3-2	CD-3
	CC3-1	CD-4
CLIN+	CD1-8	CD-5
	CD1-7	CD-6
CLIN-	CD1-6	CD-7
	CD1-5	CD-8
TXCL2-	CD1-9	CD-9
	CD1-10	CD-10
TXCL1-	CD1-11	CD-11
GND	CD1-12	CD-12
TXCL3-	CD2-13	CD-13
	CD1-14	CD-14
TXCL4-	CD1-15	CD-15
	CD1-16	CD-16
	CD1-4	CD-17
	CD1-3	CD-18
TXCLR2+	CD1-2	CD-19
	CD1-1	CD-20
TXCLR1+	CD2-8	CD-21
	CD2-7	CD-22
TXCLR3+	CD2-6	CD-23
GND	CD2-5	CD-24
TXCLR4+	CD2-9	CD-25
	CD2-10	CD-26
	CD2-11	CD-27
	CD2-12	CD-28
	CD2-13	CD-29
	CD2-14	CD-30
EXTCLK+	CD2-15	CD-31
GND	CD2-16	CD-32
SCOPESY	CD2-4	CD-33
	CD2-3	CD-34
WDTTST	CD2-2	CD-35
	CD2-1	CD-36
WDTEXS-	CE1-8	CD-37
	CE1-7	CD-38
RETOUT-	CE1-6	CD-39
	CE1-5	CD-40
EXPFI-	CE1-9	CD-41
	CE1-10	CD-42
RETIN-	CE1-11	CD-43
	CE1-12	CD-44

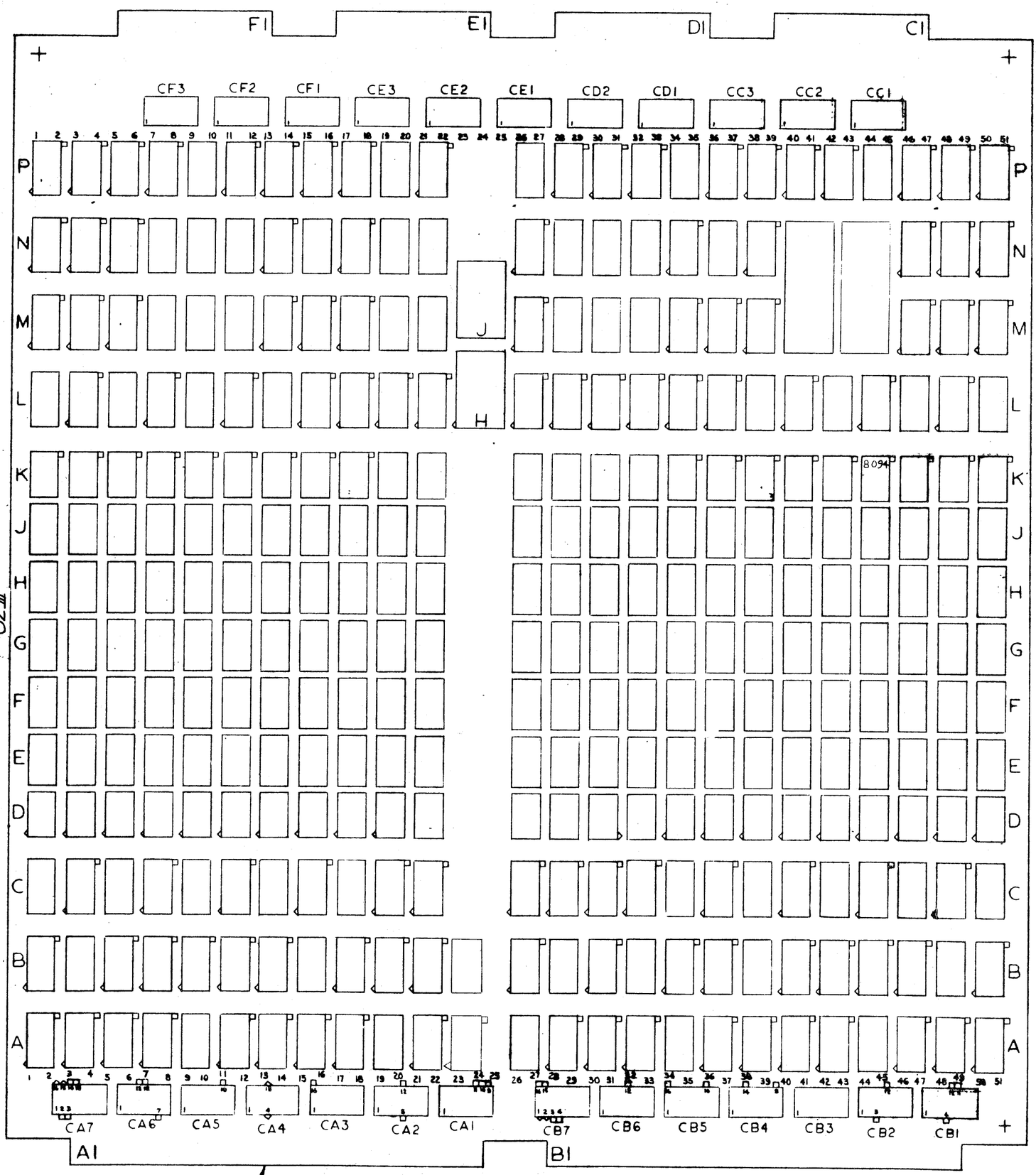
NAME	DIP SITE	CONN PIN
B20D01+	CE1-13	CE-1
GND	CE1-14	CE-2
B20D02+	CE1-15	CE-3
GND	CE1-16	CE-4
B20D03+	CE1-4	CE-5
GND	CE1-3	CE-6
B20D04+	CE1-2	CE-7
GND	CE1-1	CE-8
B20D05+	CE2-8	CE-9
GND	CE2-7	CE-10
B20D06+	CE2-6	CE-11
GND	CE2-5	CE-12
B20D07+	CE2-9	CE-13
GND	CE2-10	CE-14
B20D08+	CE2-11	CE-15
GND	CE2-12	CE-16
B20D09+	CE2-13	CE-17
GND	CE2-14	CE-18
B20D10+	CE2-15	CE-19
GND	CE2-16	CE-20
B20D11+	CE2-4	CE-21
GND	CE2-3	CE-22
B20D12+	CE2-2	CE-23
GND	CE2-1	CE-24
B20D13+	CE3-8	CE-25
GND	CE3-7	CE-26
B20D14+	CE3-6	CE-27
GND	CE3-5	CE-28
B20D15+	CE3-9	CE-29
GND	CE3-10	CE-30
B20D16+	CE3-11	CE-31
GND	CE3-12	CE-33
D2SKS	CE3-13	CE-33
GND	CE3-14	CE-34
D2MVF	CE3-15	CE-35
GND	CE3-16	CE-36
D2RDY	CE3-4	CE-37
GND	CE3-3	CE-38
D2OTA	CE3-2	CE-39
GND	CE3-1	CE-40
D2STRB	CF1-8	CE-41
GND	CF1-7	CE-42
D2MVR	CF1-6	CE-43
GND	CF1-5	CE-44

NAME	DIP SITE	CONN PIN
B10D01+	CF1-9	CF-1
GND	CF1-10	CF-2
B10D02+	CF1-11	CF-3
GND	CF1-12	CF-4
B10D03+	CF1-13	CF-5
GND	CF1-14	CF-6
B10D04+	CF1-15	CF-7
GND	CF1-16	CF-8
B10D05+	CF1-4	CF-9
GND	CF1-3	CF-10
B10D06+	CF1-2	CF-11
GND	CF1-1	CF-12
B10D07+	CF2-8	CF-13
GND	CF2-7	CF-14
B10D08+	CF2-6	CF-15
GND	CF2-5	CF-16
B10D09+	CF2-9	CF-17
GND	CF2-10	CF-18
B10D10+	CF2-11	CF-19
GND	CF2-12	CF-20
B10D11+	CF2-13	CF-21
GND	CF2-14	CF-22
B10D12+	CF2-15	CF-23
GND	CF2-16	CF-24
B10D13+	CF2-4	CF-25
GND	CF2-3	CF-26
B10D14+	CF2-2	CF-27
GND	CF2-1	CF-28
B10D15+	CF3-8	CF-29
GND	CF3-7	CF-30
B10D16+	CF3-6	CF-31
GND	CF3-5	CF-32
DISKS	CF3-9	CF-33
GND	CF3-10	CF-34
DIMVF	CF3-11	CF-35
GND	CF3-12	CF-36
DIRDY	CF3-13	CF-37
GND	CF3-14	CF-38
DIOTA	CF3-15	CF-39
GND	CF3-16	CF-40
DISTRB	CF3-4	CF-41
GND	CF3-3	CF-42
DIMVR	CF3-2	CF-43
GND	CF3-1	CF-44

MATERIAL	DWN.	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	CONNECTOR SIGNAL NAME LIST, SOC
	ENG.	
	APPRD	
USED ON / NEXT ASSY	SCALE / SHEET 24 OF	SIZE C / DWG. NO. LBD1528 / REV. A

WW

IF38

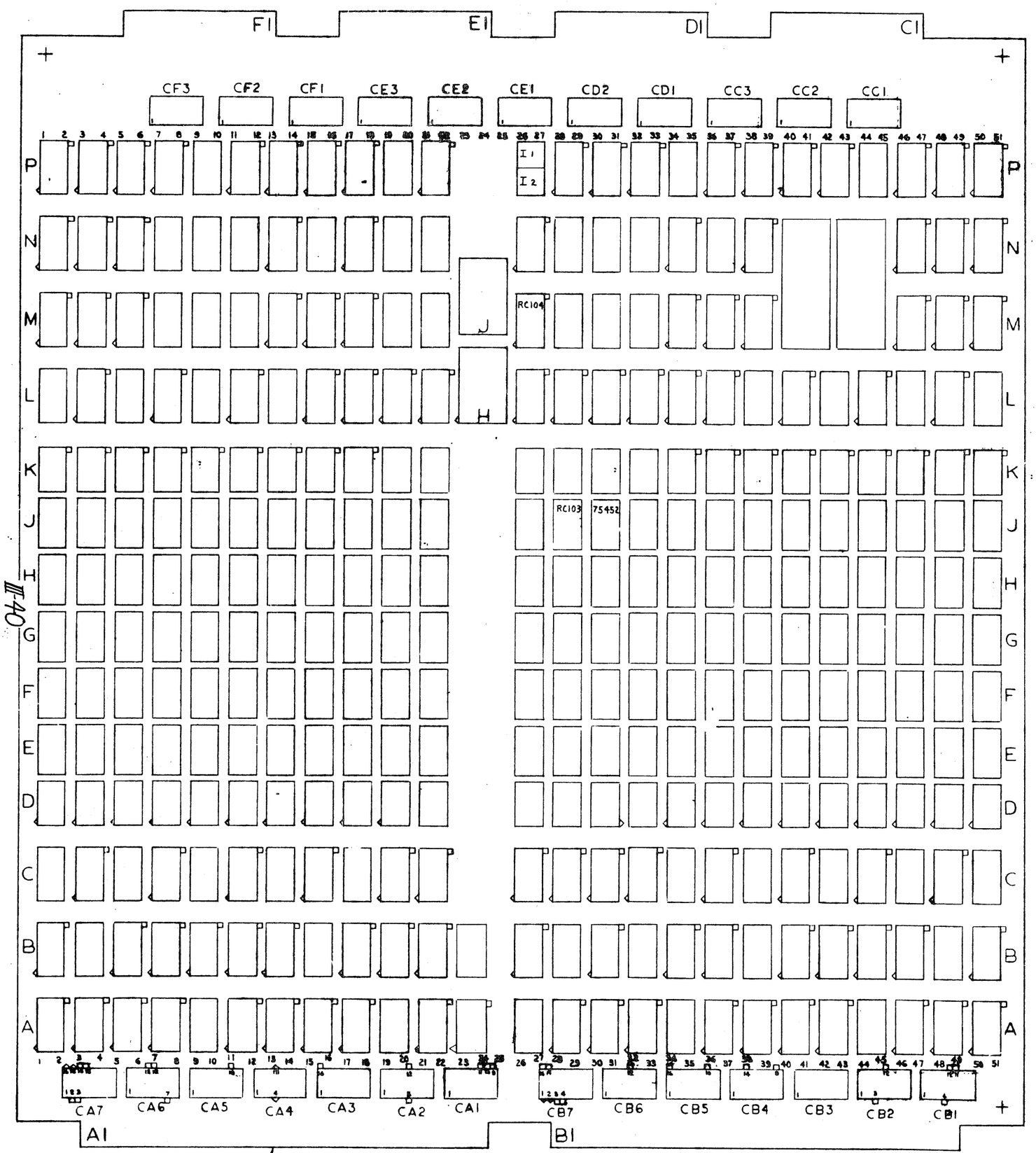


M. Bayan 5/14/74

PRIME COMPUTER INC.
NATICK, MASS.

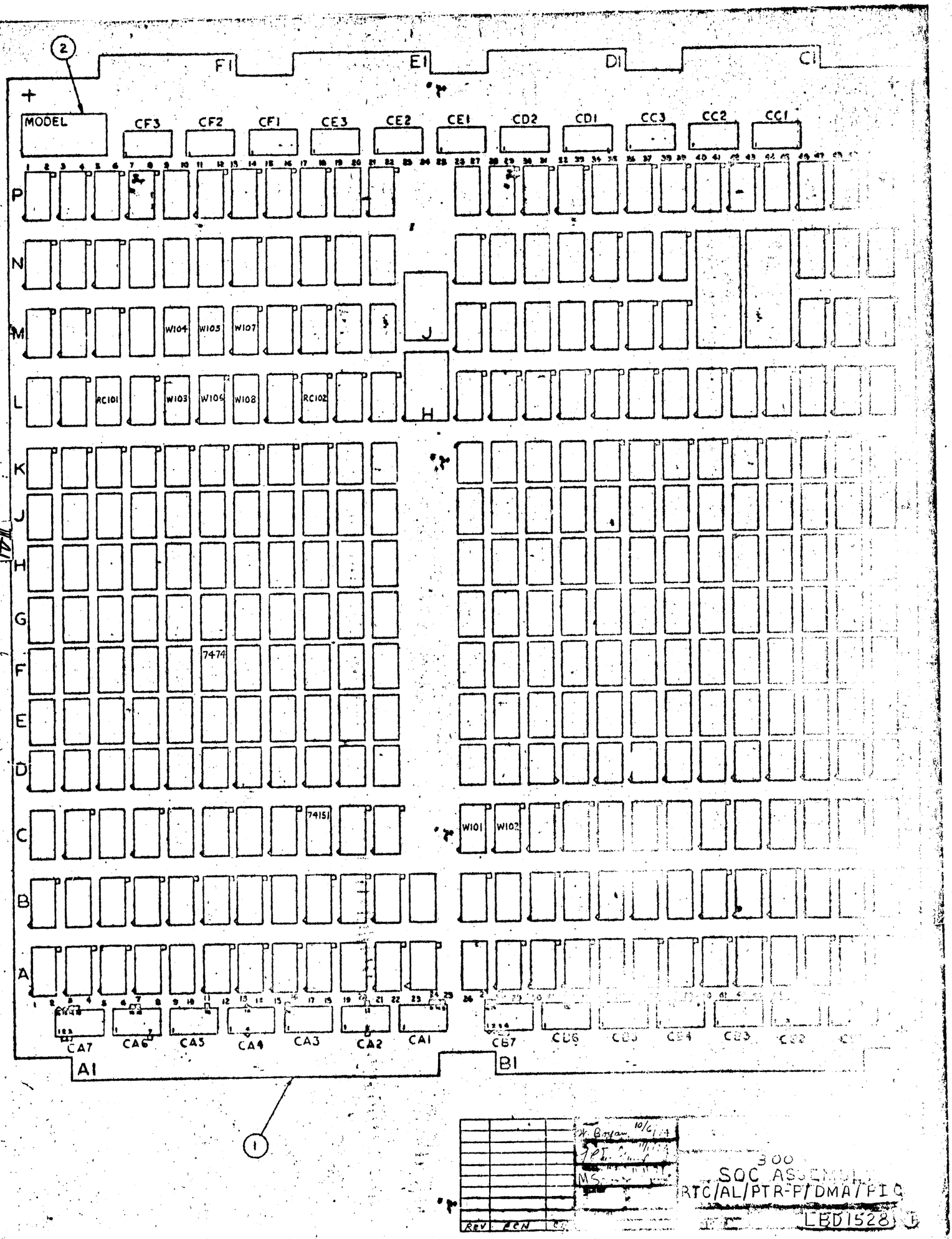
3022
SLC OPTION
SOC DIP ALLOCATION

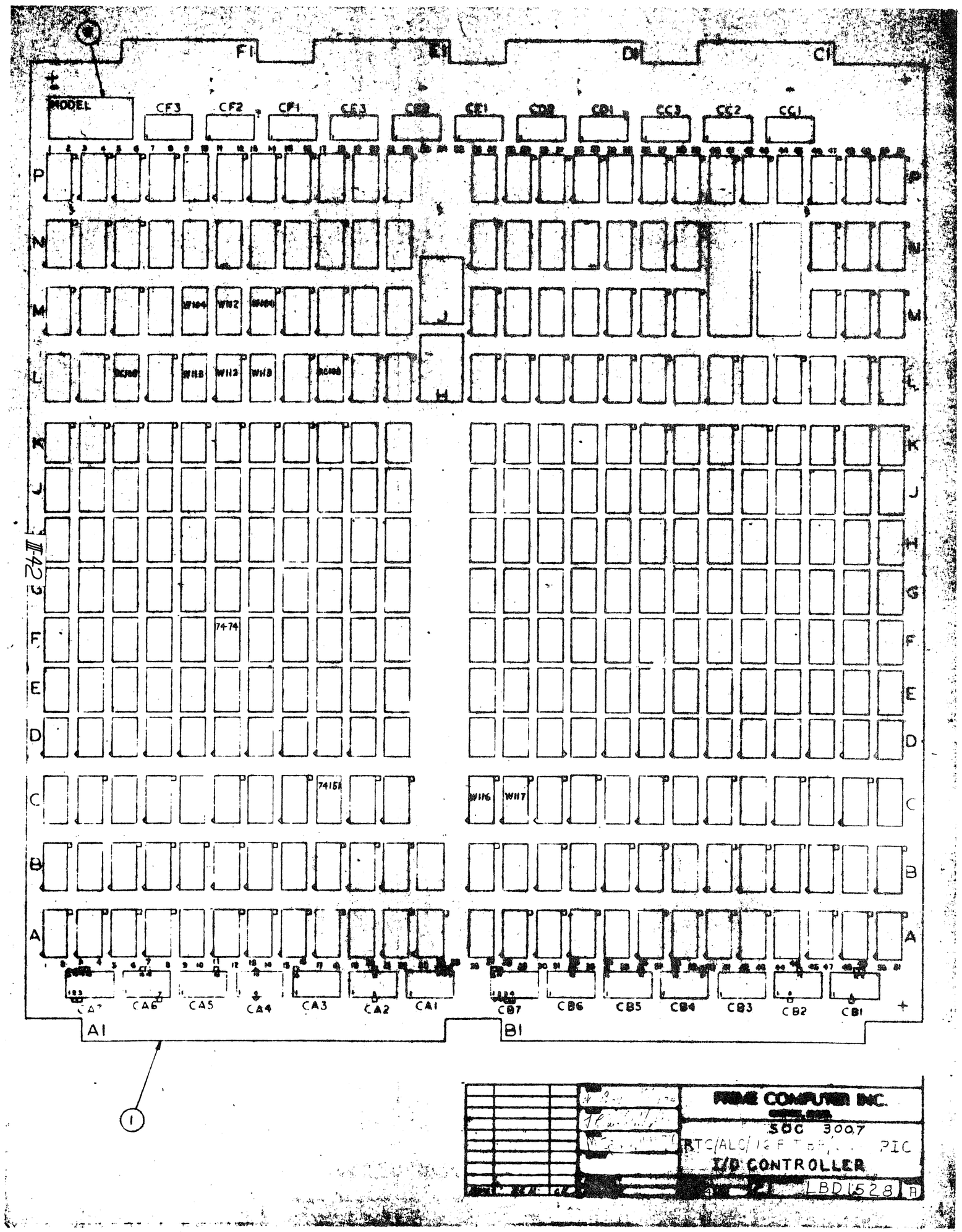
LBD1528 A



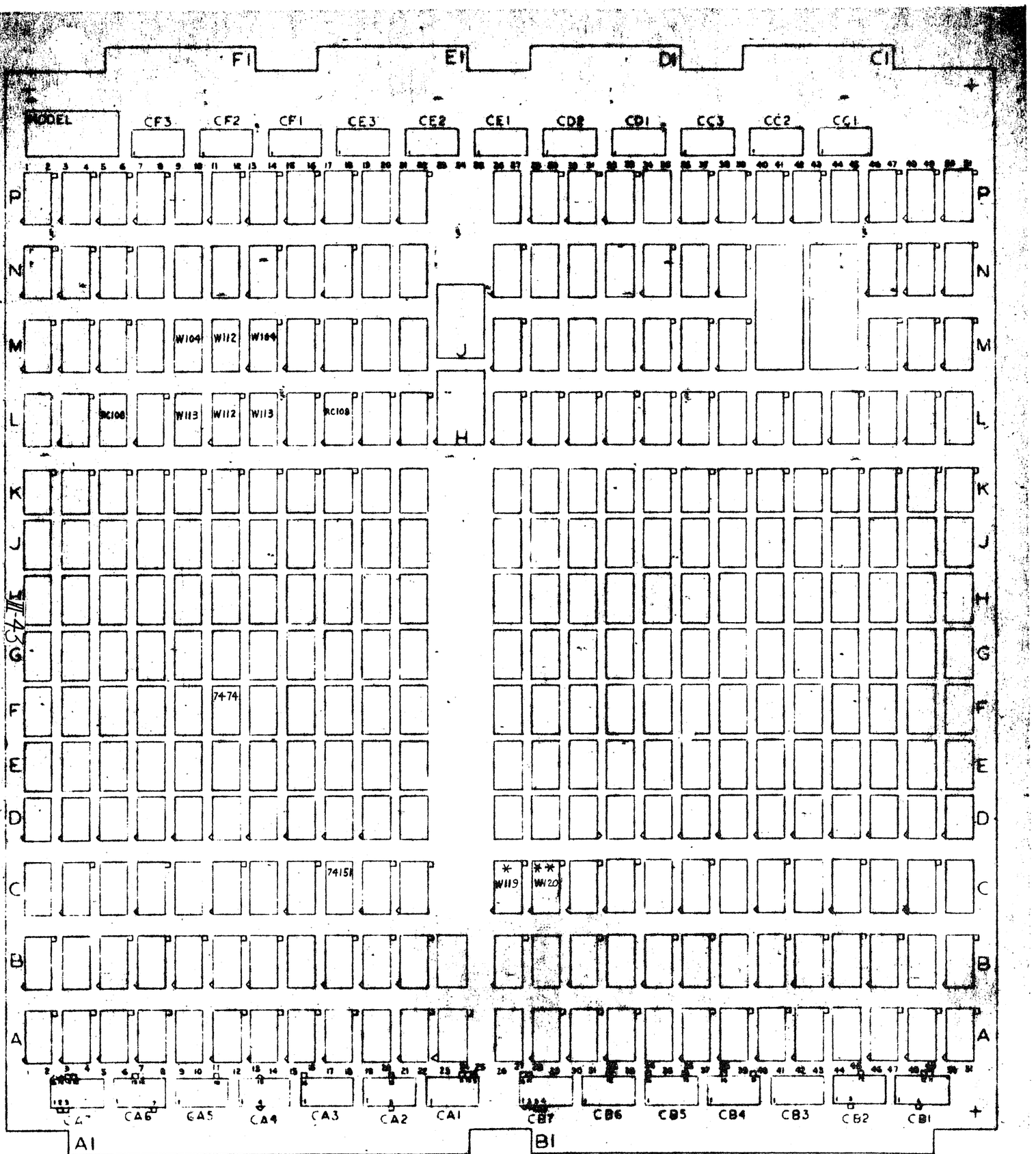
BASIC SOC ASSY
3011 THRU 3015

J Bogan 5/15/74	PRIME COMPUTER INC. FRAMINGHAM, MASS.	
	3023 WDT OPTION SOC DIP ALLOCATION	
	42	C LBD1528 A


2
F1
E1
D1
C1
MODEL
CF3
CF2
CF1
CE3
CE2
CE1
CD2
CD1
CC3
CC2
CC1
P
N
M
L
K
J
H
G
F
E
D
C
B
A
W104
W105
W107
RC101
W103
W106
W108
RC102
J
H
7474
74151
W101
W102
CA7
CA6
CA5
CA4
CA3
CA2
CA1
CB7
CB6
CB5
CB4
CB3
CB2
CB1
A1
B1
1
W. Bryan 10/6/
SPT
MS
300
SOC ASSEMBLY
RTC/AL/PTR-P/DMA/PIO
REV ECN
LED1528



	PRIME COMPUTER INC.
	SOC 300-7
	RTC/ALC/16 F T [illegible] PIC
	I/O CONTROLLER
	LBD1528 A

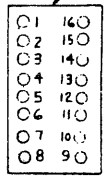


3007-001 (PRE REQUISITE)

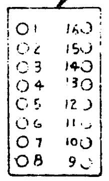
* REPLACES W116 ON 3007-001
** REPLACES W117 ON 3007-001

	W Bojan 10/7/74 Peter Glaser 11/11/74 M Soare 11-11-74	PRIME COMPUTER INC. SOC 3025 RTC/ALC/ 16 BIT BP/ SMA, PIC I/O CONTROLLER LBD1528 A

PRIME COMPUTER, INC.



HEADER DIP A
(SITE 27C)



HEADER DIP B
(SITE 29C)

HEADER DIP A — OPTIONS 3006, 3007 (ALC(TTY) & SLC)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
12	↕	1	00 - 07
12		2	10 - 17
12		3	20 - 27
12		4	30 - 37
12		5	40 - 47
12		6	50 - 57
12		7	60 - 67
12	TO	9	70 - 77

HEADER DIP A — OPTIONS 3006 (PTR) 3007 (BPIOC)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
13	↕	1	00 - 07
13		2	10 - 17
13		3	20 - 27
13		4	30 - 37
13		5	40 - 47
13		6	50 - 57
13		7	60 - 67
13	TO	9	70 - 77

HEADER DIP A — OPTIONS 3006 (PTP) 3025 (2ND BPIOC)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
14	↕	1	00 - 07
14		2	10 - 17
14		3	20 - 27
14		4	30 - 37
14		5	40 - 47
14		6	50 - 57
14		7	60 - 67
14	TO	9	70 - 77

HEADER DIP A — OPTIONS 3006, 3007 (RTC, PRTC(PIC), WDT)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
15	↕	1	00 - 07
15		2	10 - 17
15		3	20 - 27
15		4	30 - 37
15		5	40 - 47
15		6	50 - 57
15		7	60 - 67
15	TO	9	70 - 77

HEADER DIP B — OPTIONS 3006, 3007 (ALC(TTY) & SLC)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
12	↕	1	0,10,20,30,40,50,60,70
12		2	1,11,21,31,41,51,61,71
12		3	2,12,22,32,42,52,62,72
12		4	3,13,23,33,43,53,63,73
12		5	4,14,24,34,44,54,64,74
12		6	5,15,25,35,45,55,65,75
12		7	6,16,26,36,46,56,66,76
12	TO	9	7,17,27,37,47,57,67,77

FOR DEFAULT:
DEVICE ADDRESS = 04
27C-12 TO 27C-01
29C-12 TO 29C-05

HEADER DIP B — OPTIONS 3006 (PTR) 3007 (BPIOC)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
13	↕	1	0,10,20,30,40,50,60,70
13		2	1,11,21,31,41,51,61,71
13		3	2,12,22,32,42,52,62,72
13		4	3,13,23,33,43,53,63,73
13		5	4,14,24,34,44,54,64,74
13		6	5,15,25,35,45,55,65,75
13		7	6,16,26,36,46,56,66,76
13	TO	9	7,17,27,37,47,57,67,77

3006 (PTR)
FOR DEFAULT:
DEVICE ADDRESS = 01
27C-13 TO 27C-01
29C-13 TO 29C-02

3007 (BPIOC)
FOR DEFAULT:
DEVICE ADDRESS = 30
27C-13 TO 27C-02
29C-13 TO 29C-01

HEADER DIP B — OPTIONS 3006 (PTP) 3025 (2ND BPIOC)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
14	↕	1	0,10,20,30,40,50,60,70
14		2	1,11,21,31,41,51,61,71
14		3	2,12,22,32,42,52,62,72
14		4	3,13,23,33,43,53,63,73
14		5	4,14,24,34,44,54,64,74
14		6	5,15,25,35,45,55,65,75
14		7	6,16,26,36,46,56,66,76
14	TO	9	7,17,27,37,47,57,67,77

3006 (PTP)
FOR DEFAULT:
DEVICE ADDRESS = 02
27C-14 TO 27C-01
29C-14 TO 29C-03

3025 (2ND BPIOC)
FOR DEFAULT:
DEVICE ADDRESS = 31
27C-14 TO 27C-04
29C-14 TO 29C-02

HEADER DIP B — OPTIONS 3006, 3007 (RTC, PRTC(PIC), WDT)

JUMPER PIN	TO	PIN	DEVICE ADDRESS
15	↕	1	0,10,20,30,40,50,60,70
15		2	1,11,21,31,41,51,61,71
15		3	2,12,22,32,42,52,62,72
15		4	3,13,23,33,43,53,63,73
15		5	4,14,24,34,44,54,64,74
15		6	5,15,25,35,45,55,65,75
15		7	6,16,26,36,46,56,66,76
15	TO	9	7,17,27,37,47,57,67,77

FOR DEFAULT:
DEVICE ADDRESS = 20
27C-15 TO 27C-03
29C-15 TO 29C-01

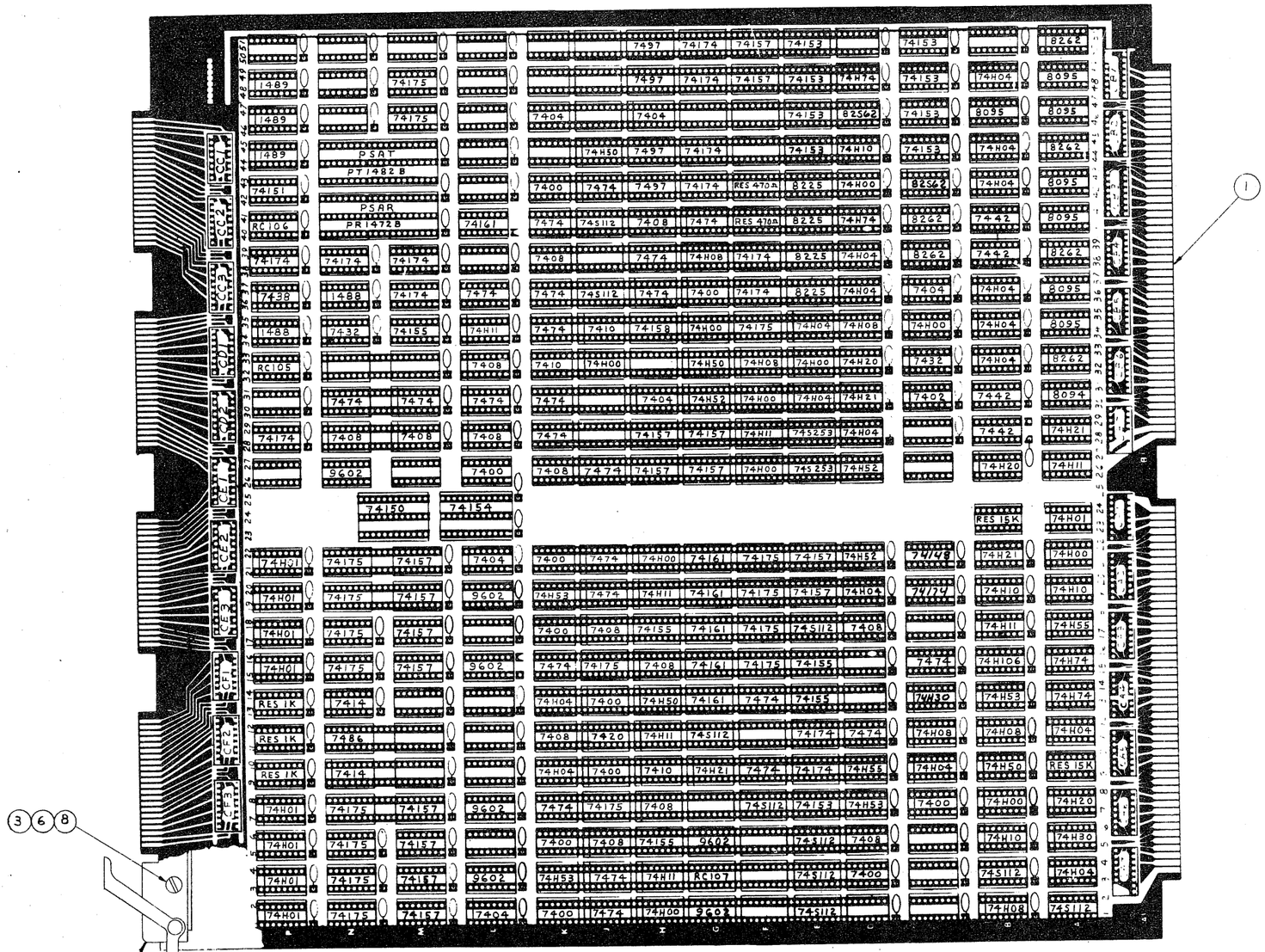
MATERIAL	
DWN	Boyan 11/8/74
CHK	11/11/74
ENG.	11-11-74
APPD	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	
USED ON	
NEXT ASSY	

PRIME COMPUTER, INC.
NATICK, MASS.

SOC
DEVICE ADDRESS
CONFIGURATION

SCALE | SHEET 4 OF | SIZE C | DWG. NO. LBD1528 | REV. A

LTR	DATE	REVISION	DR.	CK.
A	7/7/74	RELEASED W.L. 3	—	—
B	10/6/74	REVISED PER ECN'S 1459, 1461 W.L. 5	JCL	MG
C	1/9/75	REVISED TO WL REV 6 PER ECN 1523 WL REV 7 ECN 1524	WB	MG
D	3/18/75	REVISED TO WL REV 8 PER ECN 1548	WB	MS
E	5/19/75	REVISED TO WL REV 9 PER ECN 1586	WB	MS
F	8-7-75	W.L. TO REV 10 / ECN 1626	PB	MS
G	1/17/76	W.L. TO REV 11 PER ECR 1727	KTS	



PRIME COMPUTER INC
NATICK, MASS.

SOC
SUB ASSEMBLY WW

D MEC 2036-XXX G

LTR	DATE	REVISION	DR.	CK.

SHEETS

OPTION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	WIRE LIST	
SOC	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X							X	X	X				X		
VERSATEC	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	27A	28A	29A	30A	31A	32A	33A	X													X		
GOULD	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	27B	28A	29B	30B	31B	32B	33B	X													X		

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED – REMOVE ALL BURRS AND SHARP EDGES. – DIMENSIONS ARE IN INCHES – TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	DIRECTORY SOC E.V.	
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD2282 REV.
	NEXT ASSY	SHEET OF	

II-01

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
REVISION LEVEL	—	A	A	A	A	B	A																		
	A	A	A	B	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	B																								
	C																								

SHEET	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
REVISION LEVEL																									
	A	A	A	A	A	A	A	A																	
									A							A	A	A				A			
				B			B																		

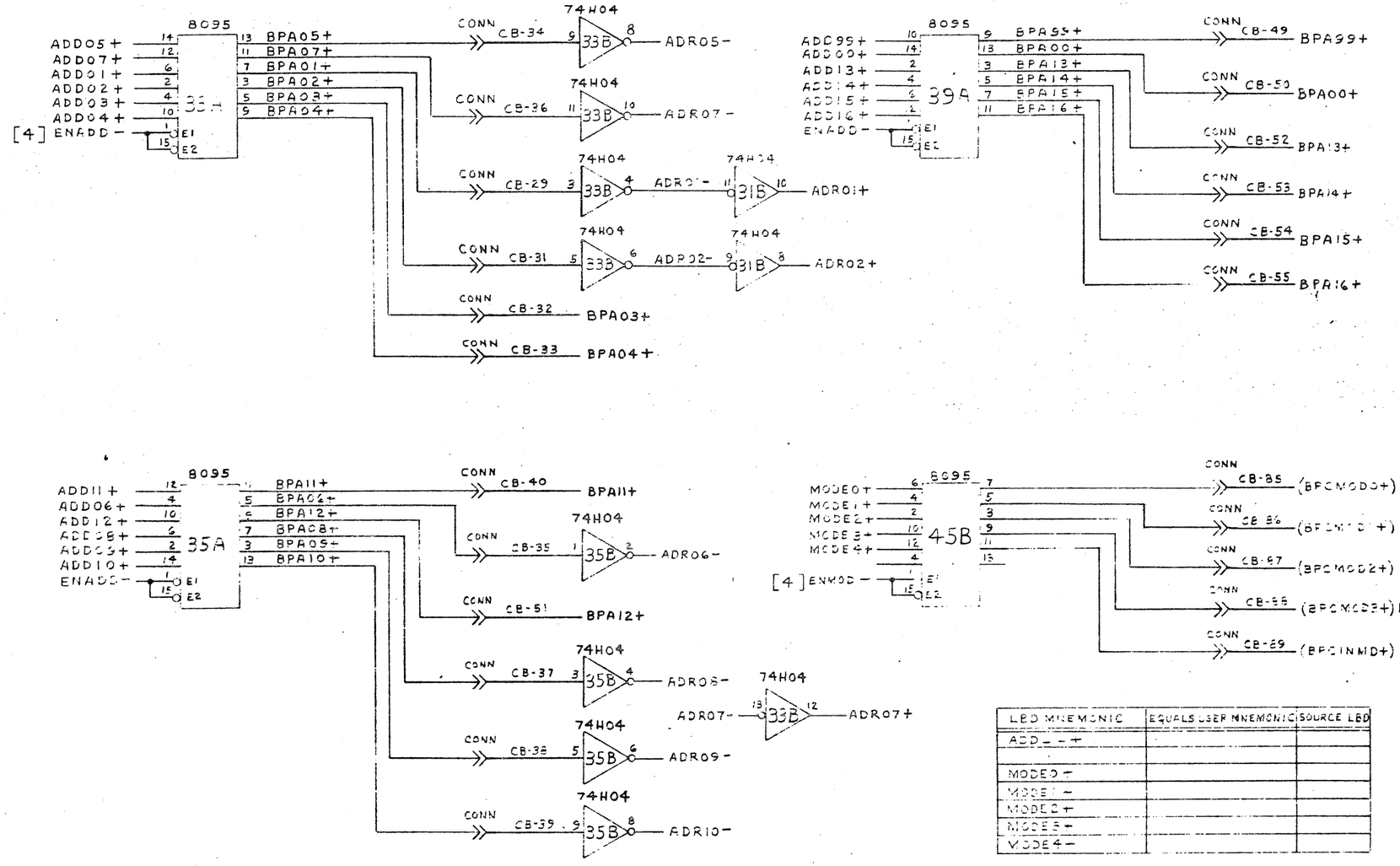
LTR	REVISION	DATE	DR.	CK.
	REVISED PER ECN 1574 (EQUAL TO W.L. REV 1 FILE NAME WWESL1)	4/21/75	[illegible]	[illegible]
	27 A, 28 A, 29 A, 30 A, 31 A, 32 A, 33 A; 27 B, 29 B, 30 B, 31 B, 32 B, 33 B — RELEASED	12/24/75	[illegible]	[illegible]
	A A A A A A A; A A A A A A — ADDED SHEETS	2/9/76	J.T.S.	
	PER ECR 1729	3/17/76	J.T.S.	[illegible]

IV-02

MATERIAL	DWN 5-15-75 Paul Beatrice	**PRIME COMPUTER, INC.** NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK [illegible] 12/24/75	REVISION STATUS SHEET SOC E.V.
	ENG. M Spoiar 12-24-75	
	APPRD	
	USED ON 3006-901	SCALE — SIZE C — DWG. NO. LBD 2282 — REV. C
	NEXT ASSY ESA 2057-901	SHEET 1 OF

REV. A — DWG. NO. LBD 2282

PRIME COMPUTER, INC.



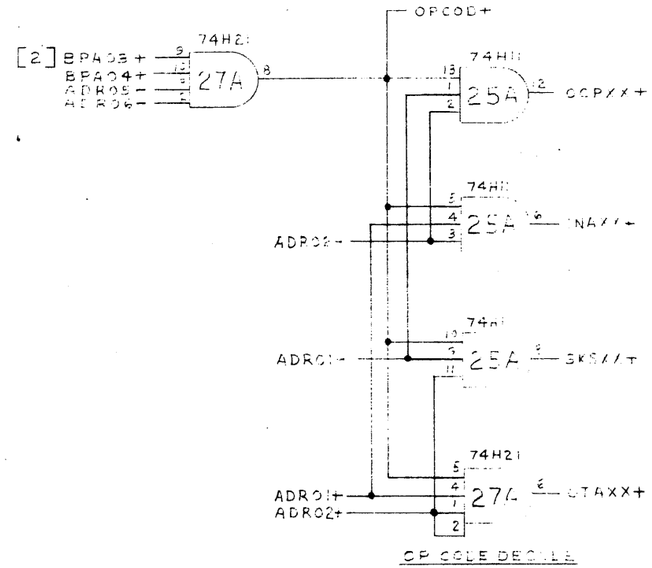
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD_ _+		
MODE0+		
MODE1−		
MODE2+		
MODE3−		
MODE4−		

I/O BUS ADDRESS
DRIVERS & RECEIVERS

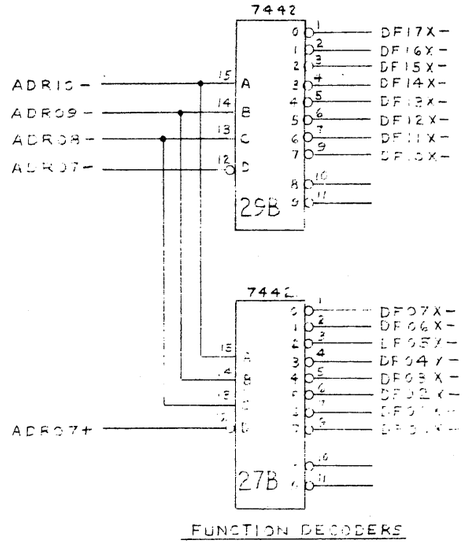
II-03

MATERIAL	DWN 3/4/77	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS AND MODE LINES
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD 2282 REV. A
NEXT ASSY	SHEET 1 OF	

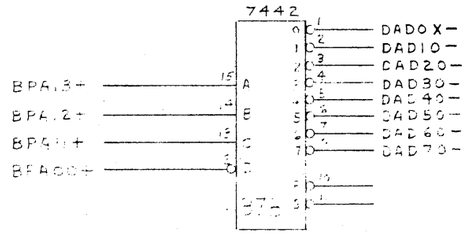
PDF-003

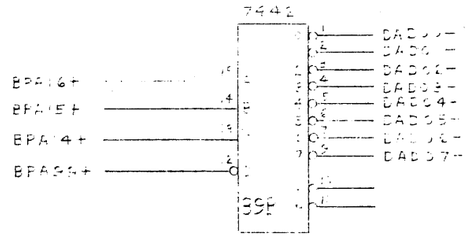


OP CODE DECODE

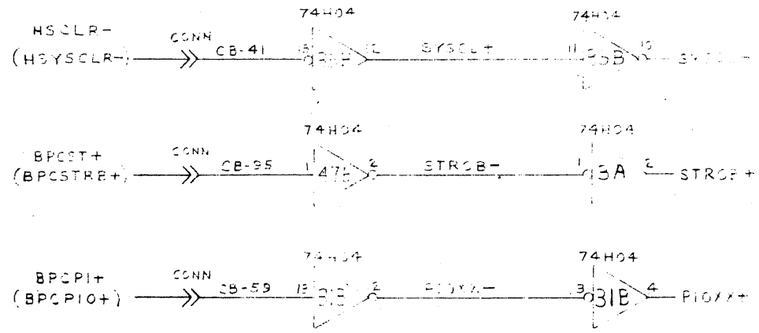


FUNCTION DECODERS





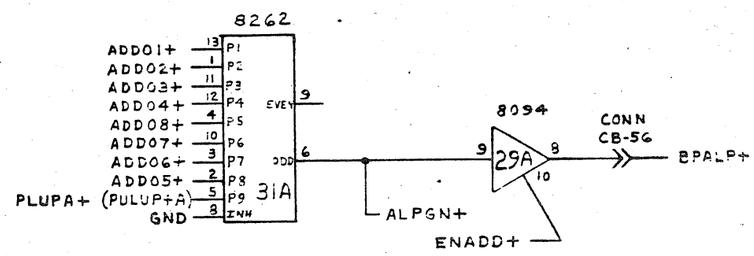
OCTAL ADDRESS DECODERS

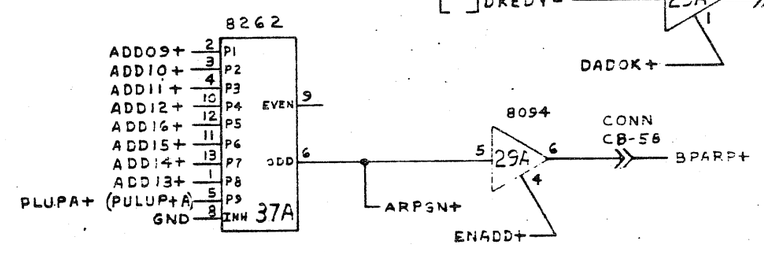


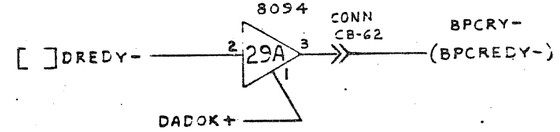
MATERIAL	DWN W. K. Tsay 3/14/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS DECODING	
	APPRD		EV
	USED ON	SCALE	SIZE C DWG. NO. LBD 2282 REV. A
	NEXT ASSY	SHEET 3 OF	

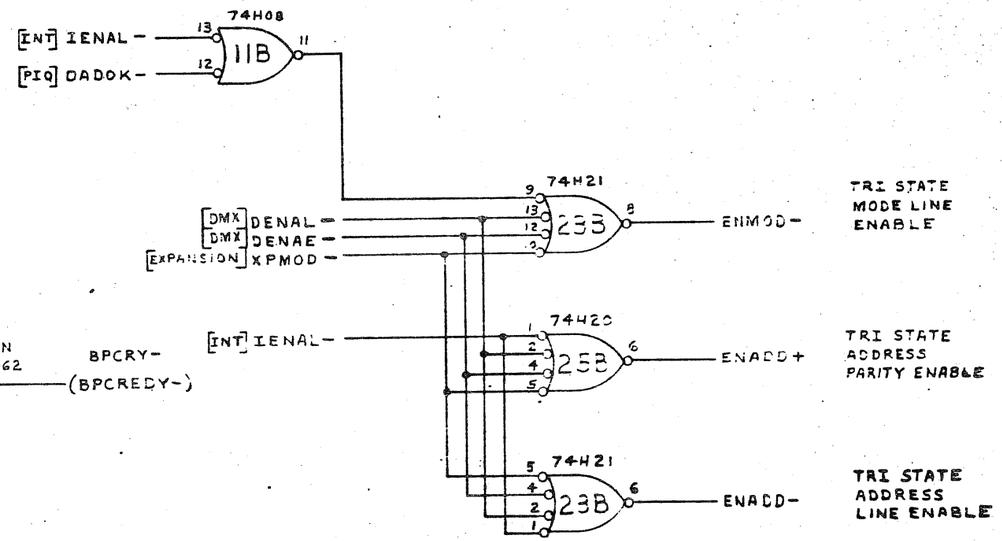
II-04

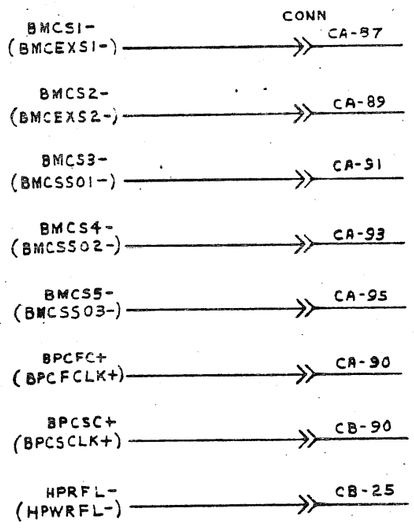
PDF-003



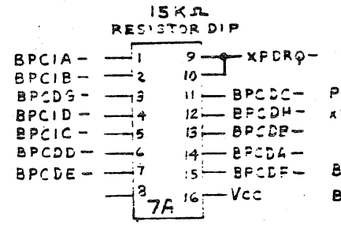


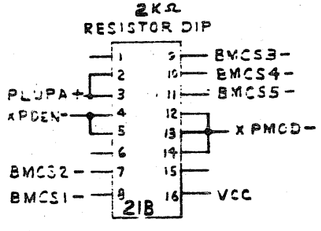






LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
COCMD+		
ADD__+		
DADOK-		
XPMOD-		
XPDEN-		
INAOK-		
CTAOK+		
XPDEE-		
DREDY-		
DADOK+		

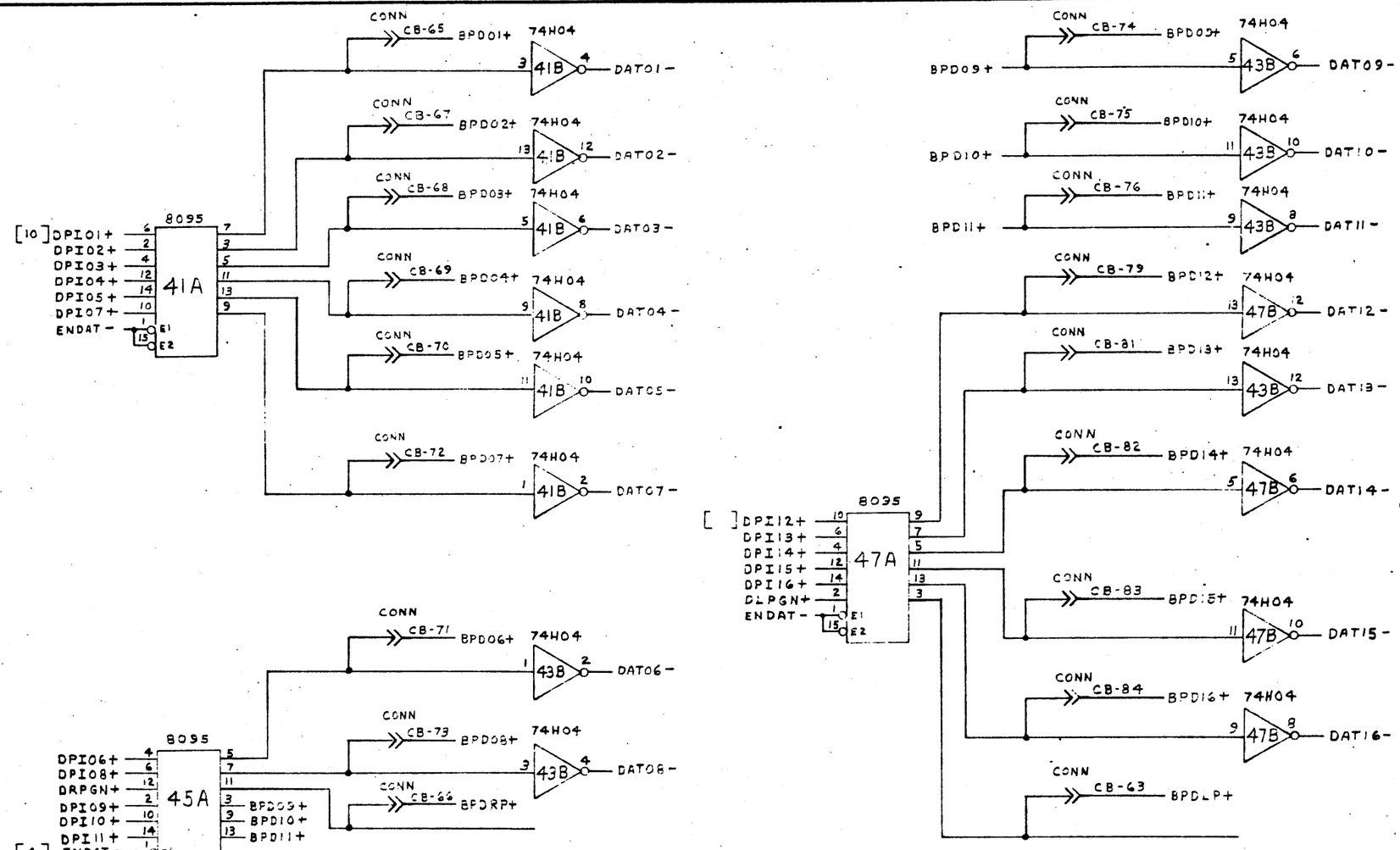




11105

MATERIAL	DWN 3/4/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS PARITY	
	APPRD		EV
	USED ON / NEXT ASSY	SCALE / SHEET 4 OF	SIZE C / DWG. NO. LBD2282 / REV. B

PDF-003



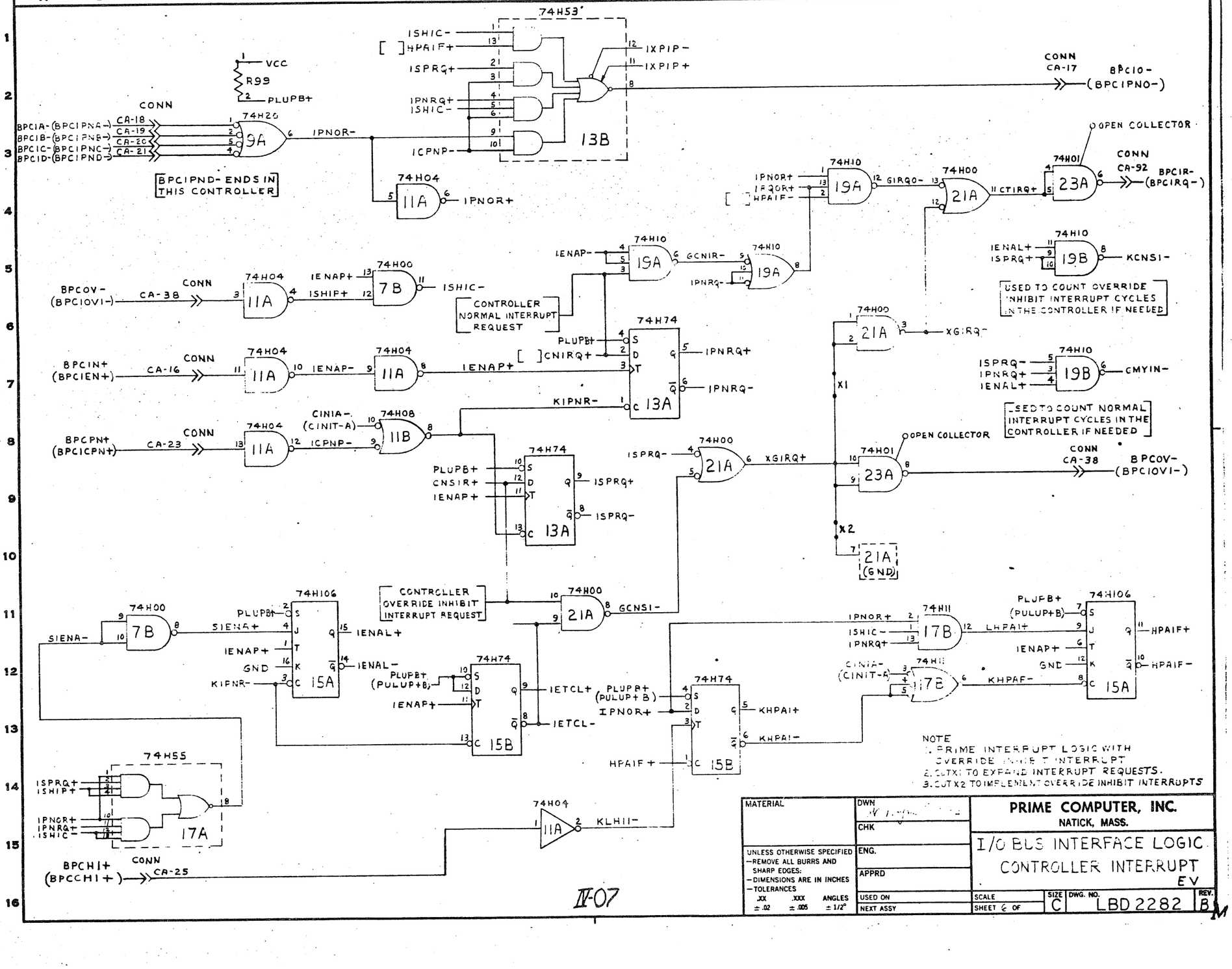
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
DPI +		

N-06

MATERIAL	DWN dr fagan 3/5/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC DATA BUS LINES EV
	ENG.	
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD 2282 REV. A
NEXT ASSY	SHEET 5 OF	

PDF-003

PRIME COMPUTER, INC.



II-07

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	I/O BUS INTERFACE LOGIC CONTROLLER INTERRUPT EV
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 6 OF
		SIZE C / DWG. NO. LBD 2282 / REV. B

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

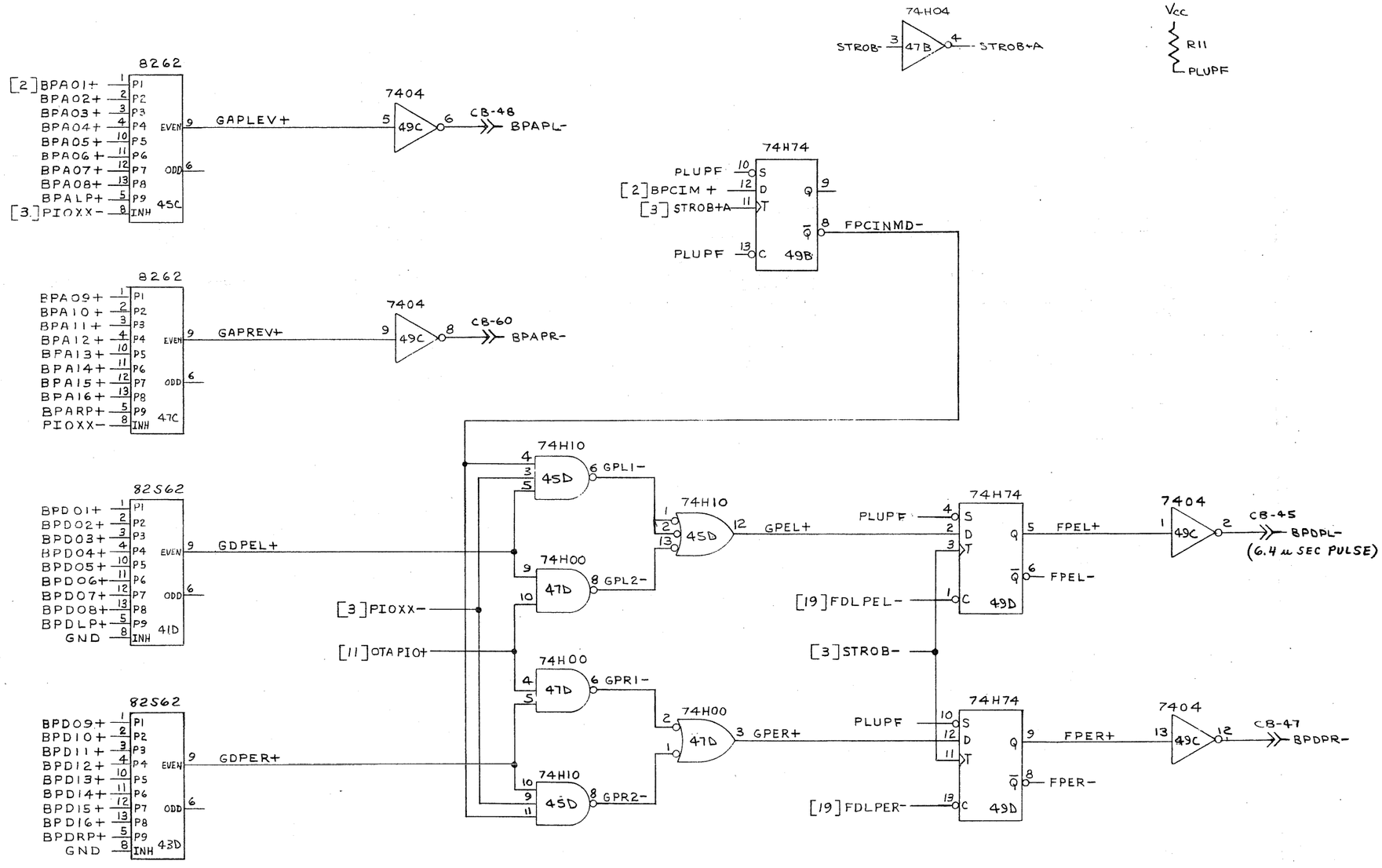
BPCDA- (BPCDPNA-)
BPCDB- (BPCDPNB-)
BPCDC- (BPCDPNC-)
BPCDD- (BPCDPND-)
BPCDE- (BPCDPNE-)
BPCDF- (BPCDPNF-)
BPCDG- (BPCDPNG-)
BPCDH- (BPCDPNH-)
CONN CA-8 CA-9 CA-10 CA-11 CA-12 CA-13 CA-14 CA-15
74H30 5A
BPCDH- (BPCDPNH-) ENDS IN THIS CONTROLLER
DPNDR-
74H04 3A
DPNDR+
74H10 5B
DENAE-
DENAP-
74S112 3B
CINIA- (CINIT-A)
PLUPB+ (PULUP+B)
DENAP-
GND
DENAL-
DENAL+
USED TO CLEAR CONTROLLER DMA/DMC REQUEST ON L.E. DENAL+ MAY BE USED TO CLEAR L.E. TRIGGERED FLIP FLOPS
CONTROLLER DMA/DMC REQUEST
74H08 1B
CNDRQ+
CNRER-
SDPNR+
CONTROLLER END OF RANGE
74S112 1A
PLUPB+ (PULUP+B)
DPNRQ+
DPNRQ-
KDPNR-
GND
74H04 3A
BPCDN+ (BPCDEN+)
CONN CA-5
DENAP-
CONTROLLER INITIALIZE
74H08 1B
CINIA- (CINIT-A)
DCPNP- 9
74H04 3A
BPCDP+ (BPCDCPN+)
CONN CA-4
DCPNP-
74H04 3A
DCPNP+
74H50 9B
DCPNP-
DCPNP-
DXPIP+ [EXPANSION]
DXPIP-
CONN CA-7 BPCDO- (BPCDPNO-)
74H00 7B
DENAP-
DMARQ-
VCC 7A
EXPANSION XPDRQ-
74H10 5B
74H01 23A
OPEN COLLECTOR
CONN CA-34 BPCDR- (BPCDRQ-)
DMA STROBE TO CONTROLLER
74H08 11B
DENDL+
MYDST+
74H10 5B
STROBE+
CERDO+
MYIDE-
BPCER+ (BPCEOR+)
CONN CA-3
CA5-14
74H08 1B
DENAL+
CDEOR+
74S112 1A
PLUPB+ (PULUP+B)
GND
DEOER+
DEOER-
CONTROLLER DMX INPUT COMMAND DECODED
CINIA- (CINIT-A)
CEORA-
74H08 1B
KDEOR-
CONTROLLER CLEAR END OF RANGE
74S112 3B
PLUPB+ (PULUP+B)
DENAL+
STROB-
GND
DENDL+
DENDL-
74H00 7B
DENDL+
[3] STROB-
KDEDL-

LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIA- (CINIT-A)		
CEORA-		
CNPER-		
CERDO+		
CNDRQ+		
XPDRQ+		

IV-08

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ± .02 XXX ± .005 ANGLES ± 1/2°	ENG.	I/O BUS INTERFACE LOGIC DMX LOGIC EV
	APPRD	
	USED ON	SCALE SIZE C DWG. NO. LBD2282
	NEXT ASSY	SHEET 7 OF

PDF-003

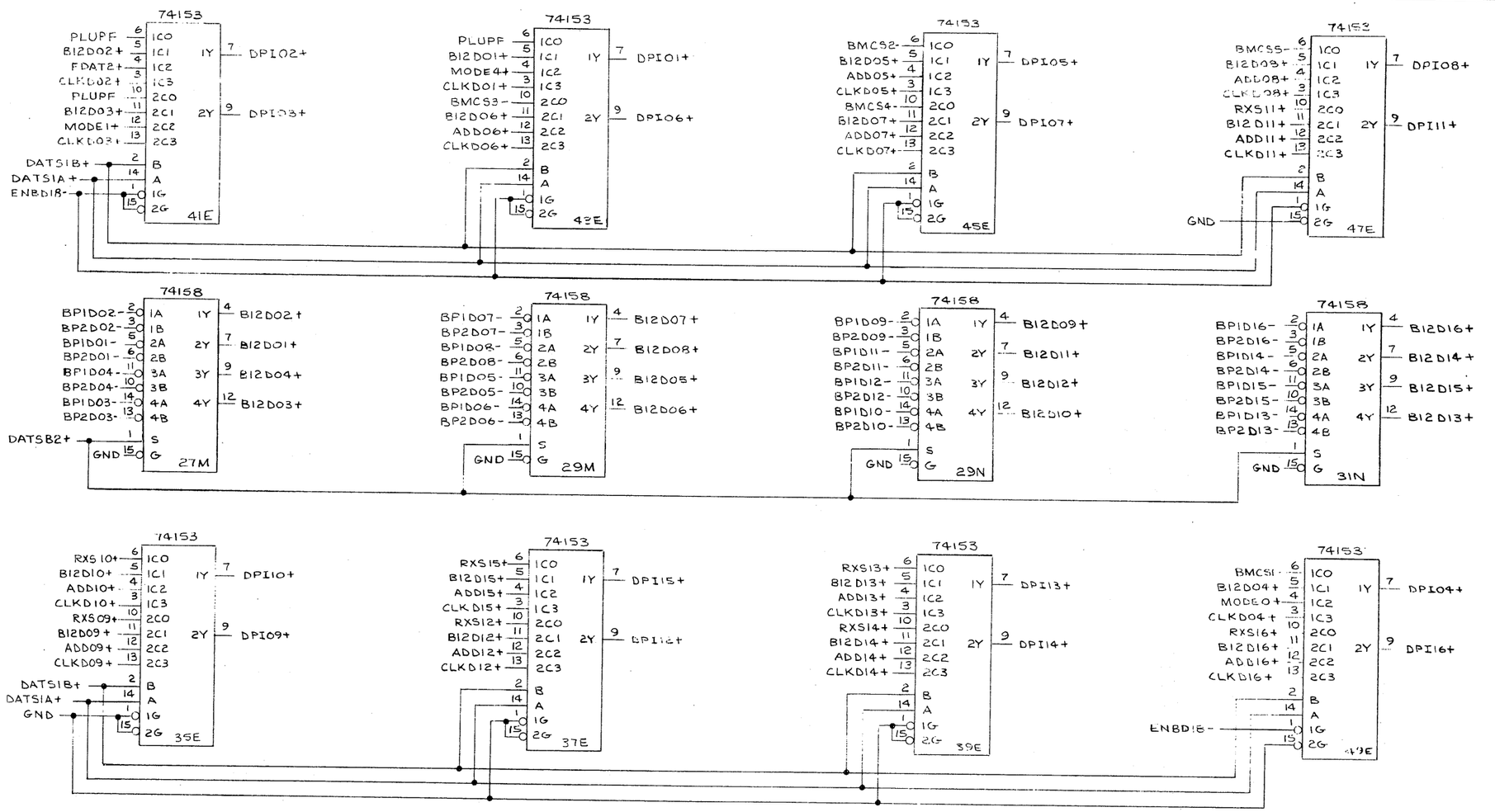


MATERIAL	DWN Paul Beatrice 5-15-75	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC I/O BUS {ADDRESS / DATA} PARITY CHECK
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 8 OF / SIZE C / DWG. NO LBD2282 / REV A

IV-09

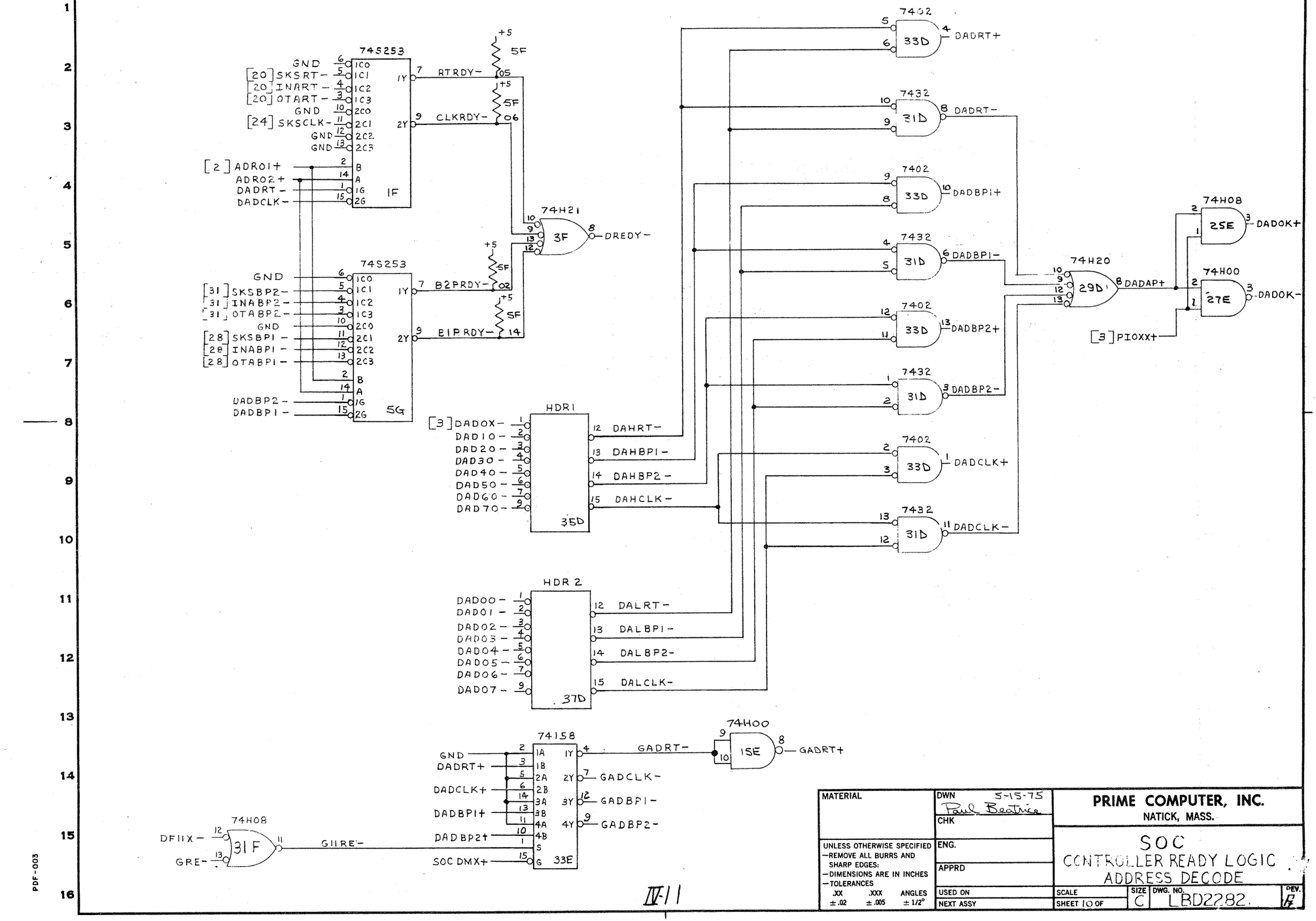
PDF-003

PRIME COMPUTER, INC.



MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC DATA MUX		
	ENG.			
	APPRD			
	USED ON	SCALE	SIZE C	DWG. NO. LBD2282 REV. A
	NEXT ASSY	SHEET 9 OF		

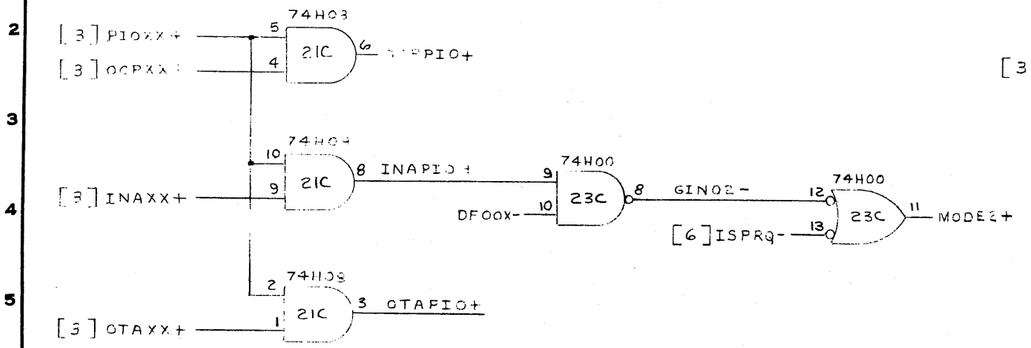
PDF-003

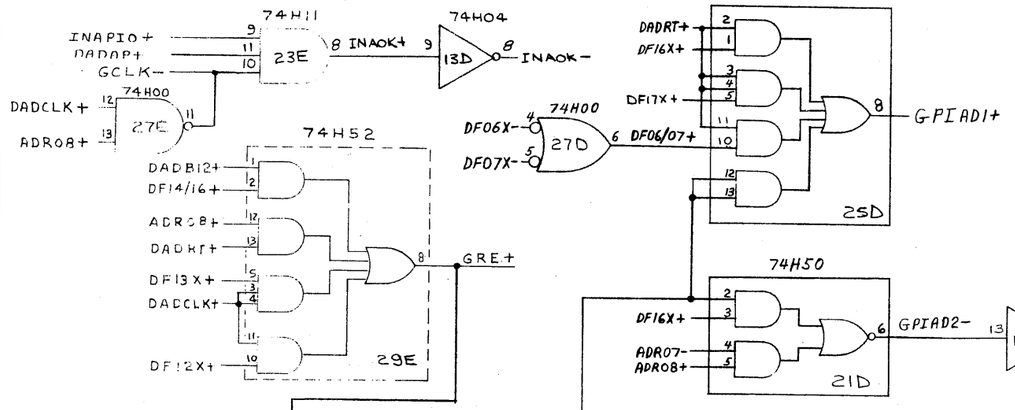


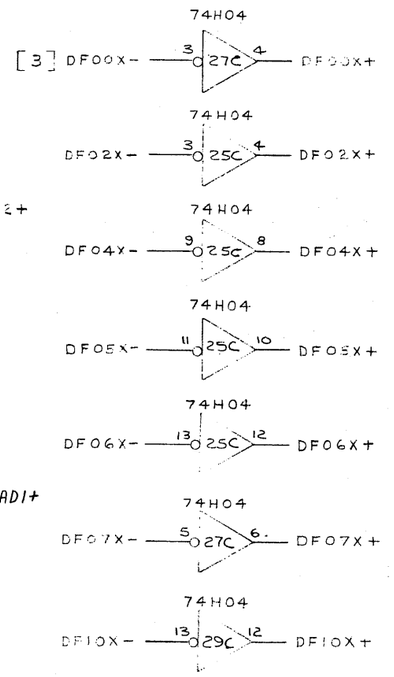
MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC CONTROLLER READY LOGIC ADDRESS DECODE	
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 10 OF	SIZE C / DWG. NO. LBD2282 / REV. 17

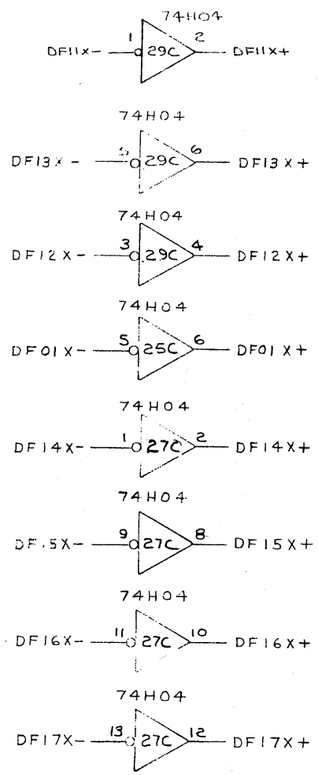
PDF-003

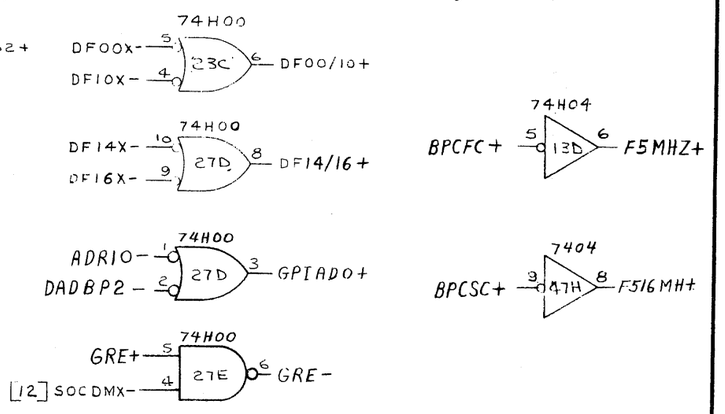
PRIME COMPUTER, INC.









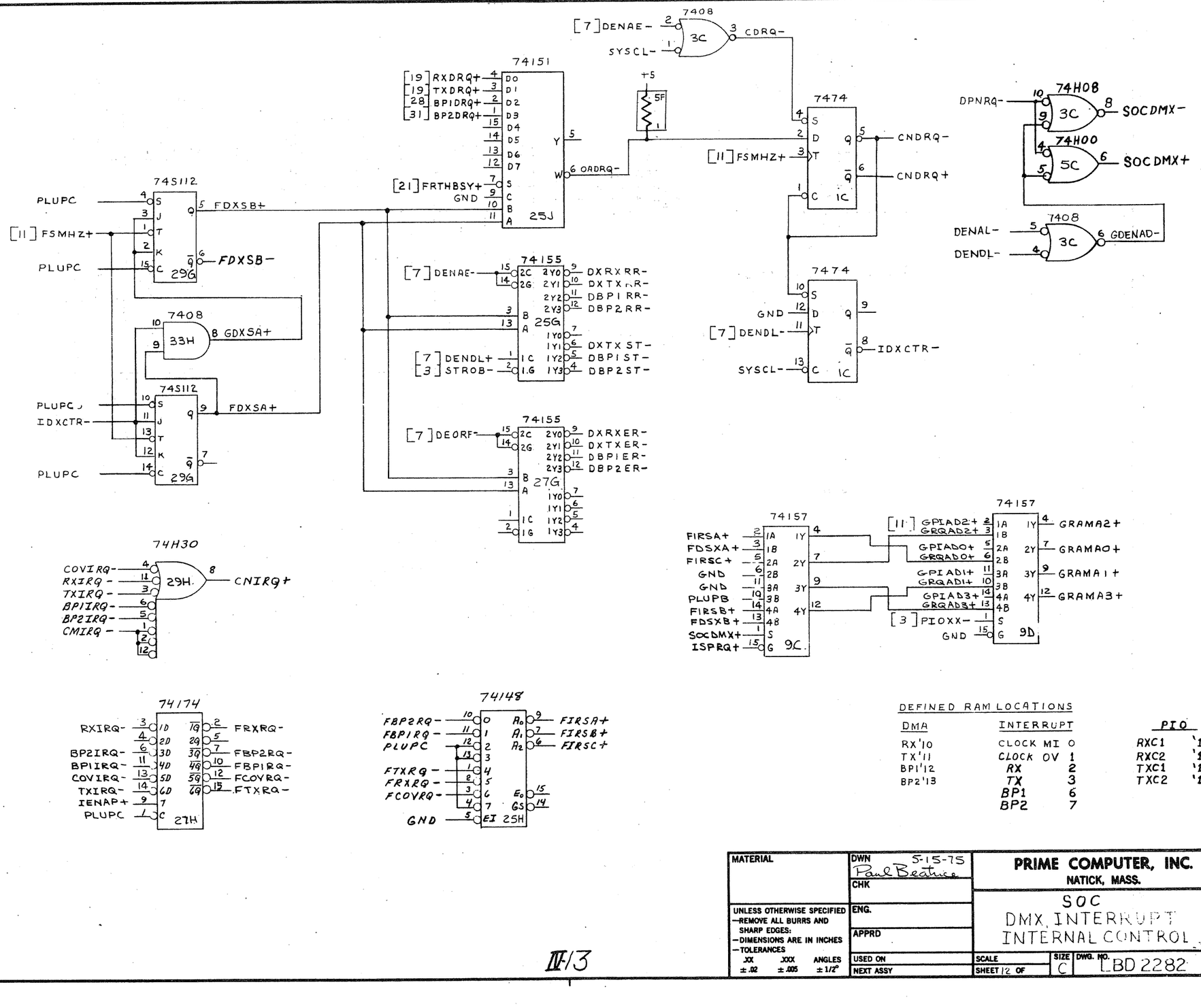


MATERIAL	DWN 5-15-15 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC MISC I/L BUS RECEIVERS
	APPRD	
	USED ON	SCALE — SIZE C DWG. NO. LRD2282 REV. A
	NEXT ASSY	SHEET 11 OF

IV-12

PDF-003

PRIME COMPUTER, INC.



DEFINED RAM LOCATIONS

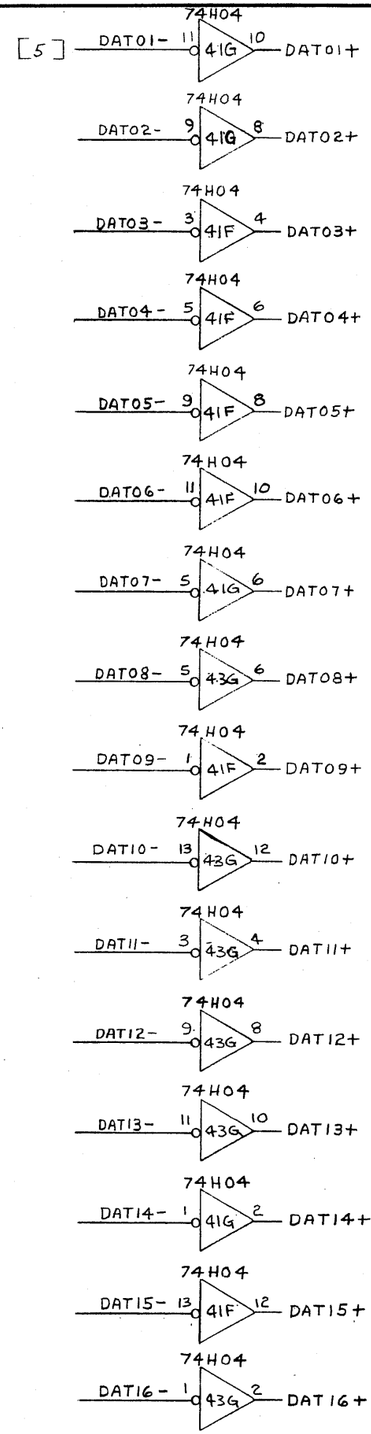
DMA	INTERRUPT		PIO	
RX '10	CLOCK MI	0	RXC1	'14
TX '11	CLOCK OV	1	RXC2	'15
BP1 '12	RX	2	TXC1	'16
BP2 '13	TX	3	TXC2	'17
	BP1	6		
	BP2	7		

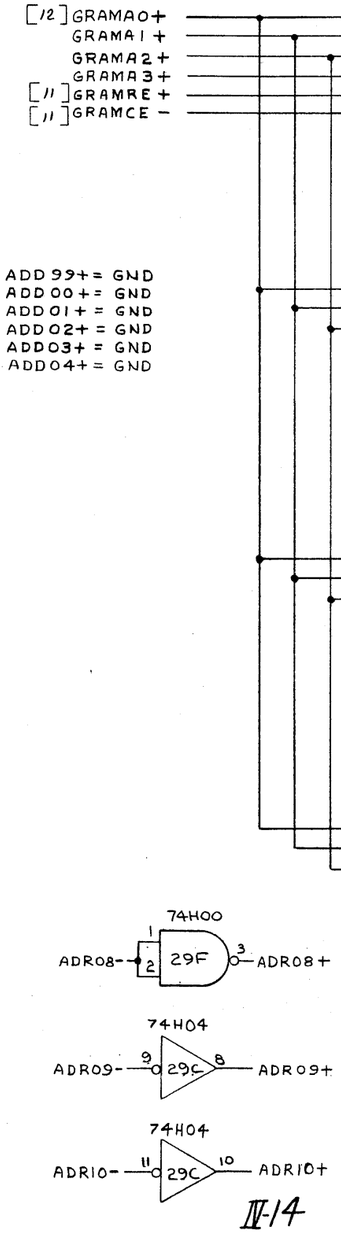
MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	SOC DMX INTERRUPT INTERNAL CONTROL	
	ENG.		
	APPRD		
USED ON / NEXT ASSY	SCALE	SIZE C	DWG. NO. LBD 2282 REV. A1
	SHEET 12 OF		

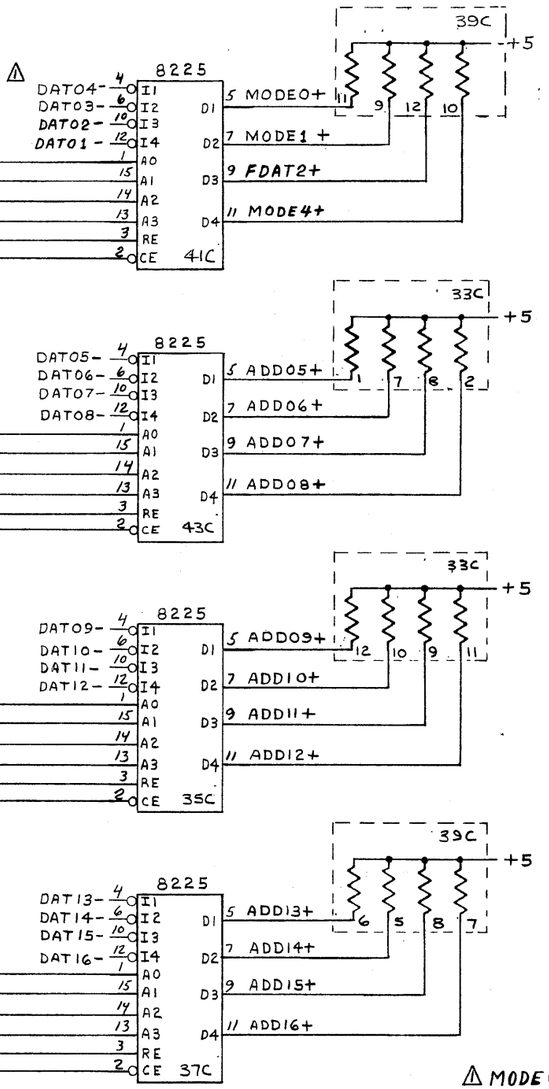
PDF-003

IV-13

PRIME COMPUTER, INC.



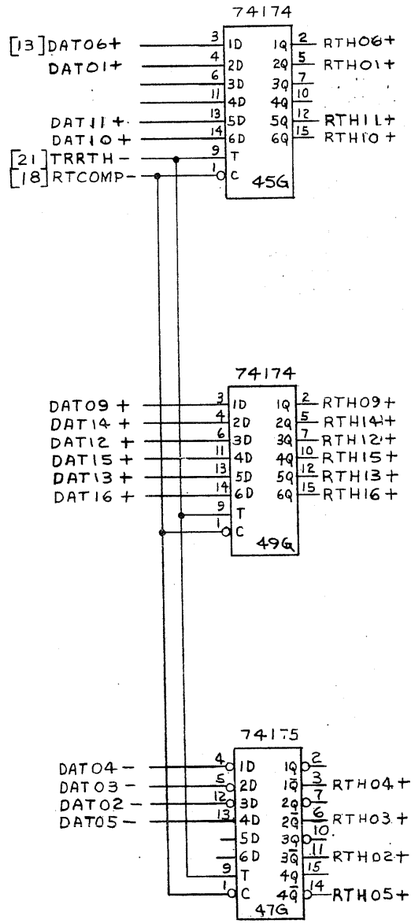


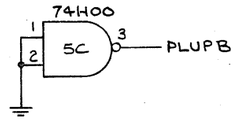


⚠ MODE 0-1 = 00 ESCAPE
01 DMT
10 DMA
11 DMC

MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC DMX INTERRUPT RAM
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF / SIZE C / DWG. NO. LBD2232 / REV. P

PDF-003

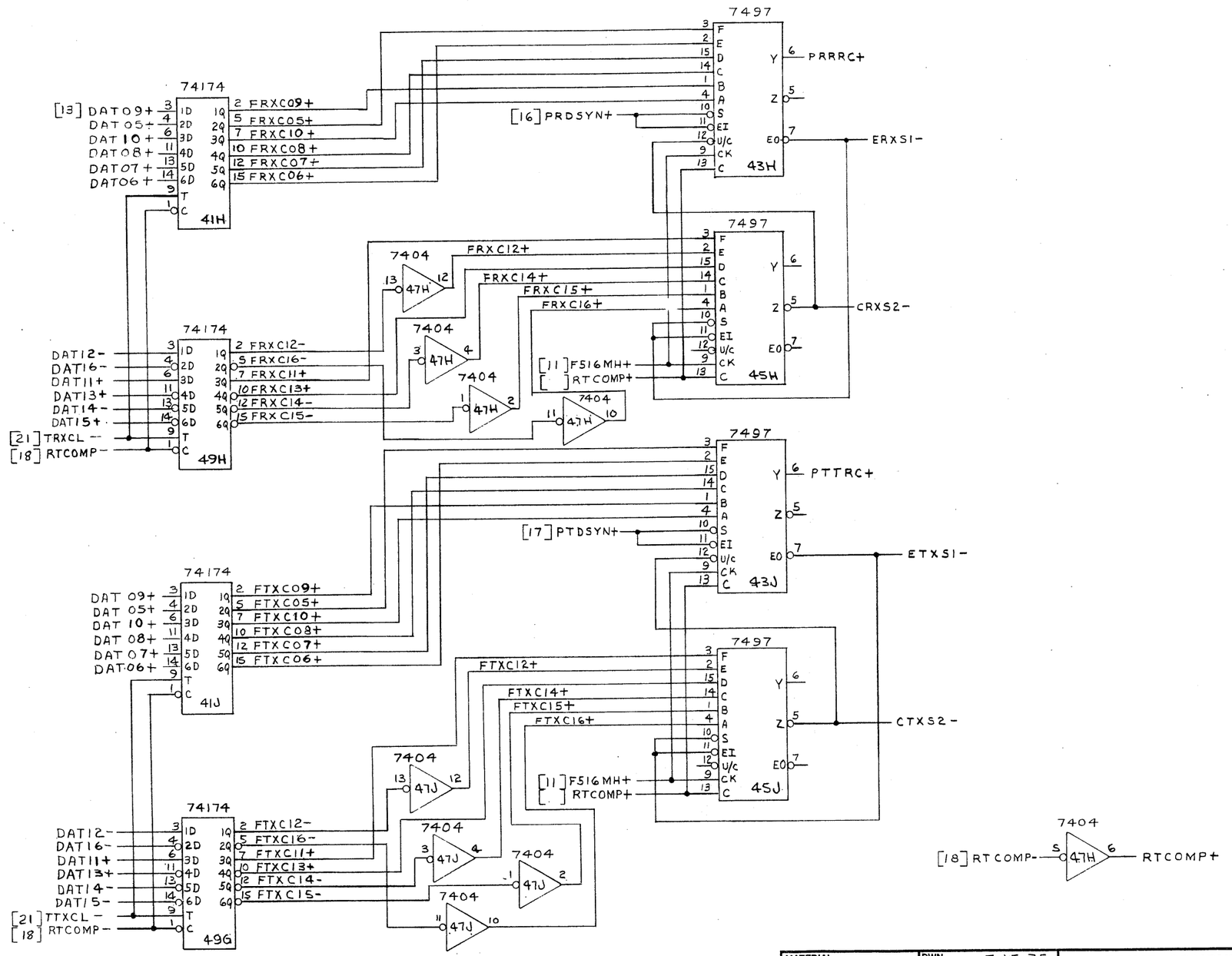




IV-15

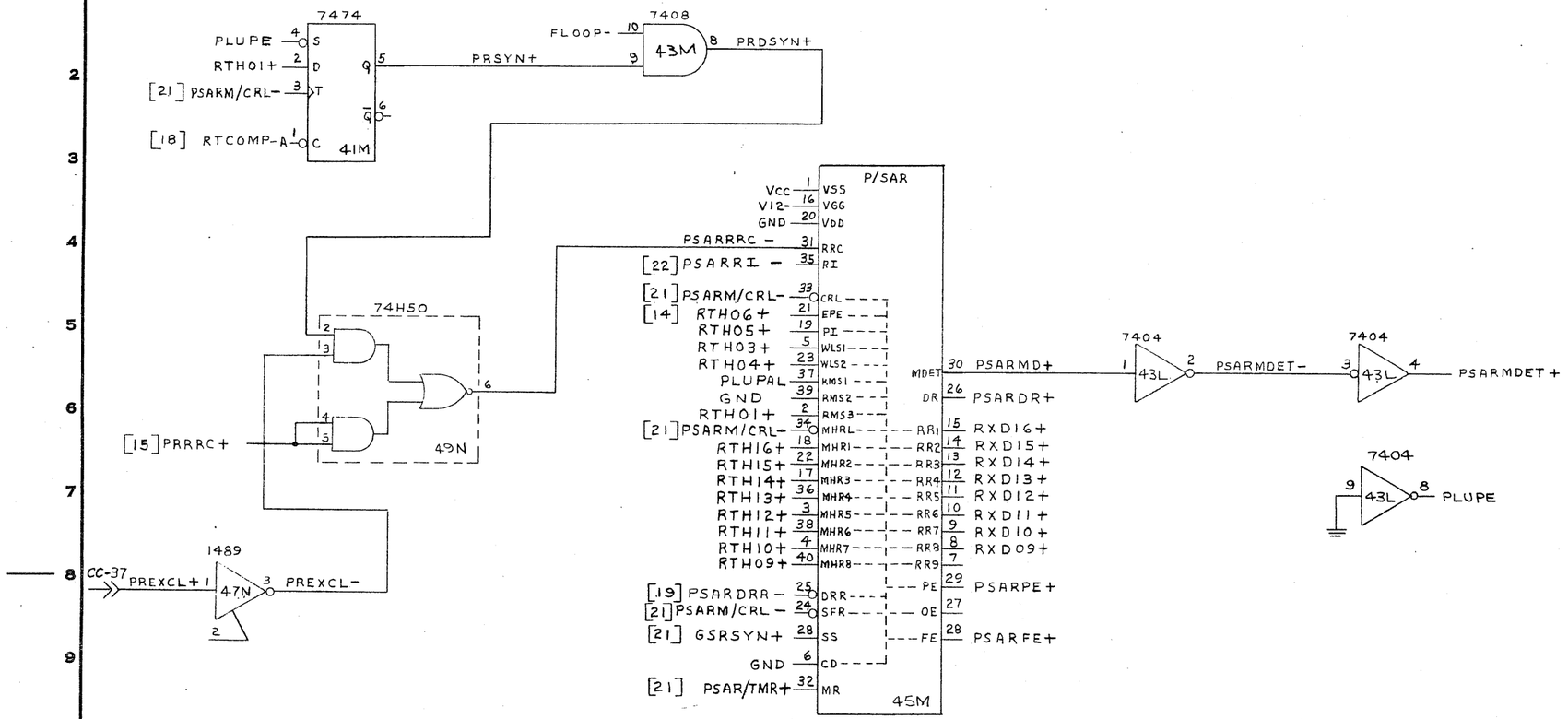
MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	SOC RT HOLDING REG	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.		
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 14 OF	SIZE C / DWG. NO. LBD 2282 / REV. H

PDF-003



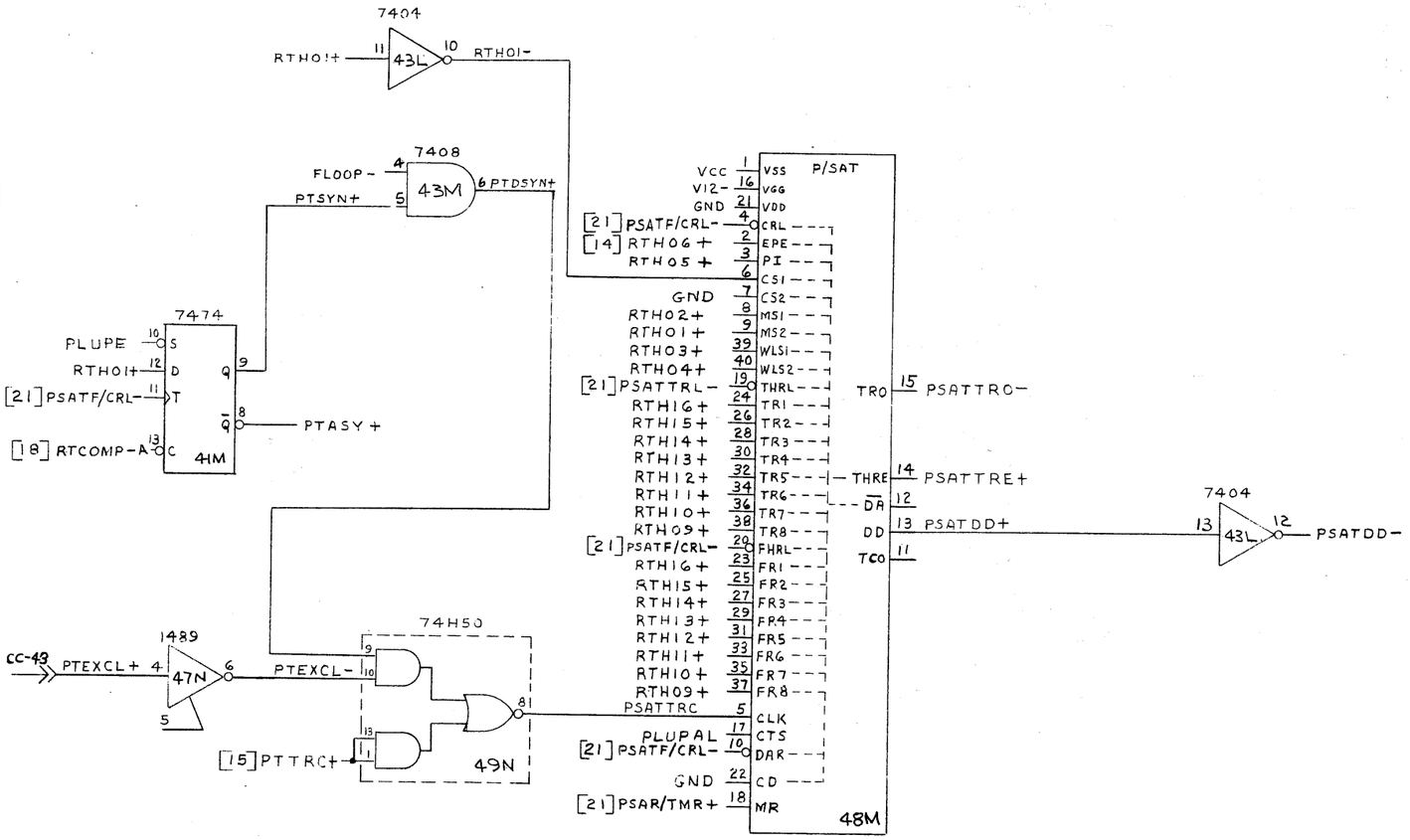
MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC RX TX BAUD CLOCK	
	ENG.		
	APPRD		
USED ON NEXT ASSY	SCALE SHEET 15 OF	SIZE C	DWG. NO. LBD2282 REV. H

PDF-003



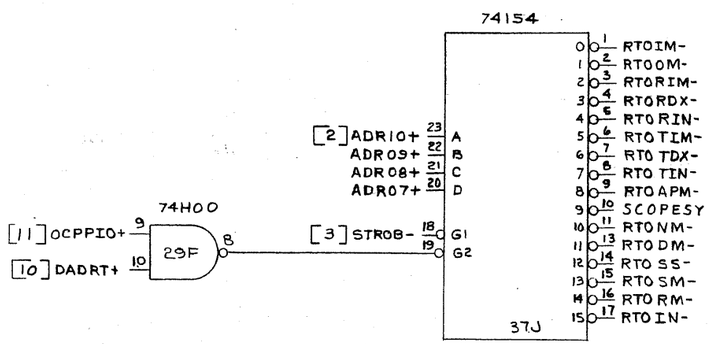
MATERIAL	DWN 5-15-75 Paul Bastrica	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	SOC PSAR	
	ENG.		
	APPRD		
	USED ON	SCALE	SIZE C
	NEXT ASSY	SHEET 16 OF	DWG. NO. LBD2232 REV. A

PDF-003



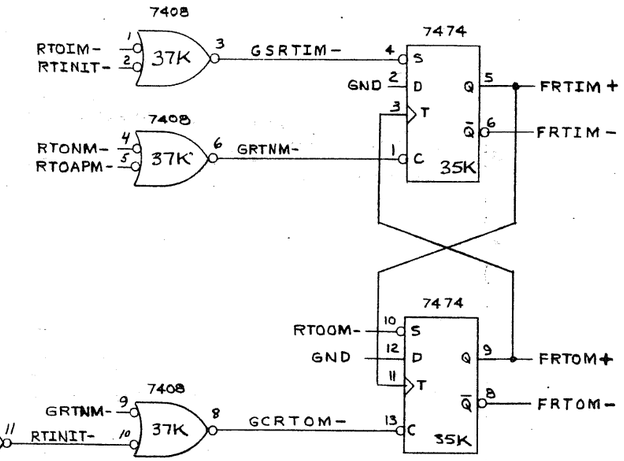
MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	SOC P SAT
	APPRD	
	USED ON	SCALE / SIZE C / DWG. NO. LBD2282 / REV. A
	NEXT ASSY	SHEET 17 OF

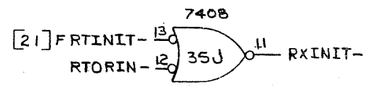
PDF-003

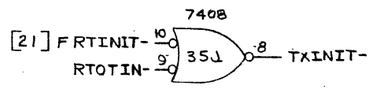


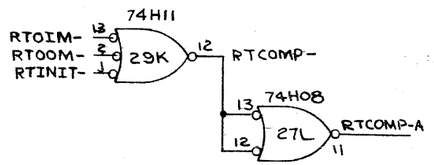
OCP

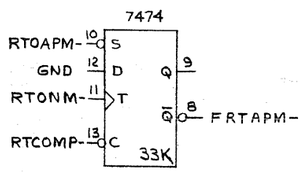
SET
- INPUT MODE
- OUTPUT MODE
- RX INTERRUPT MODE
- RX DMX MODE
- RX INITIALIZE
- TX INTERRUPT MODE
- TX DMX MODE
- TX INITIALIZE
- A' MODE
- — DIAGNOSTIC SYNC
- NORMAL MODE
- DIAGNOSTIC
- SEARCH FOR SYNC
- SET RT INTERRUPT MODE
- RESET RT INTERRUPT MODE
- RT INIT[illegible]IZE

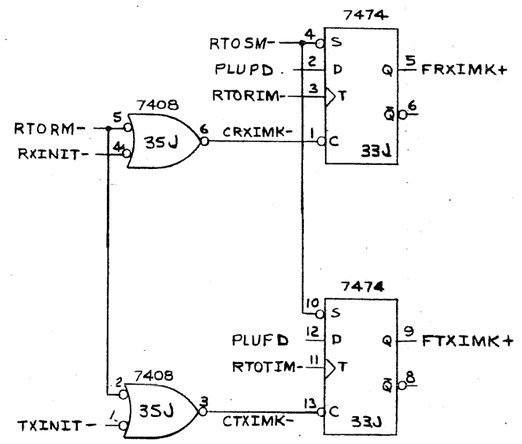


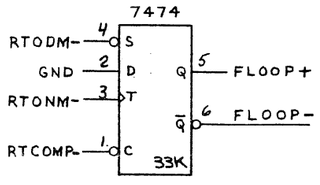






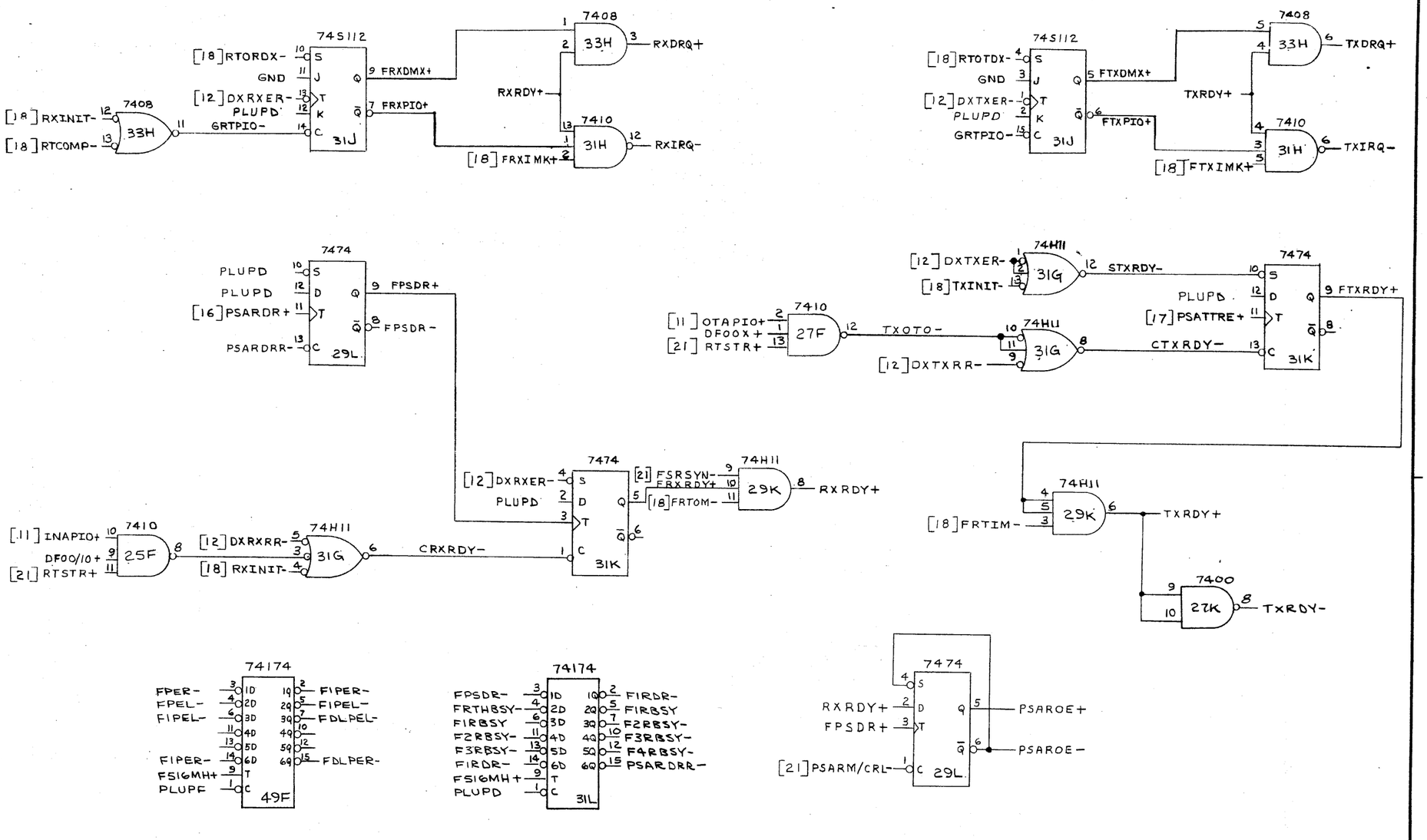






MATERIAL	DWN 3-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC RX/TX I/O CONTROL
	APPRD	
	USED ON / NEXT ASSY	SCALE — / SHEET 18 OF
		SIZE C / DWG. NO. LBD2282 / REV. A

PDF-003

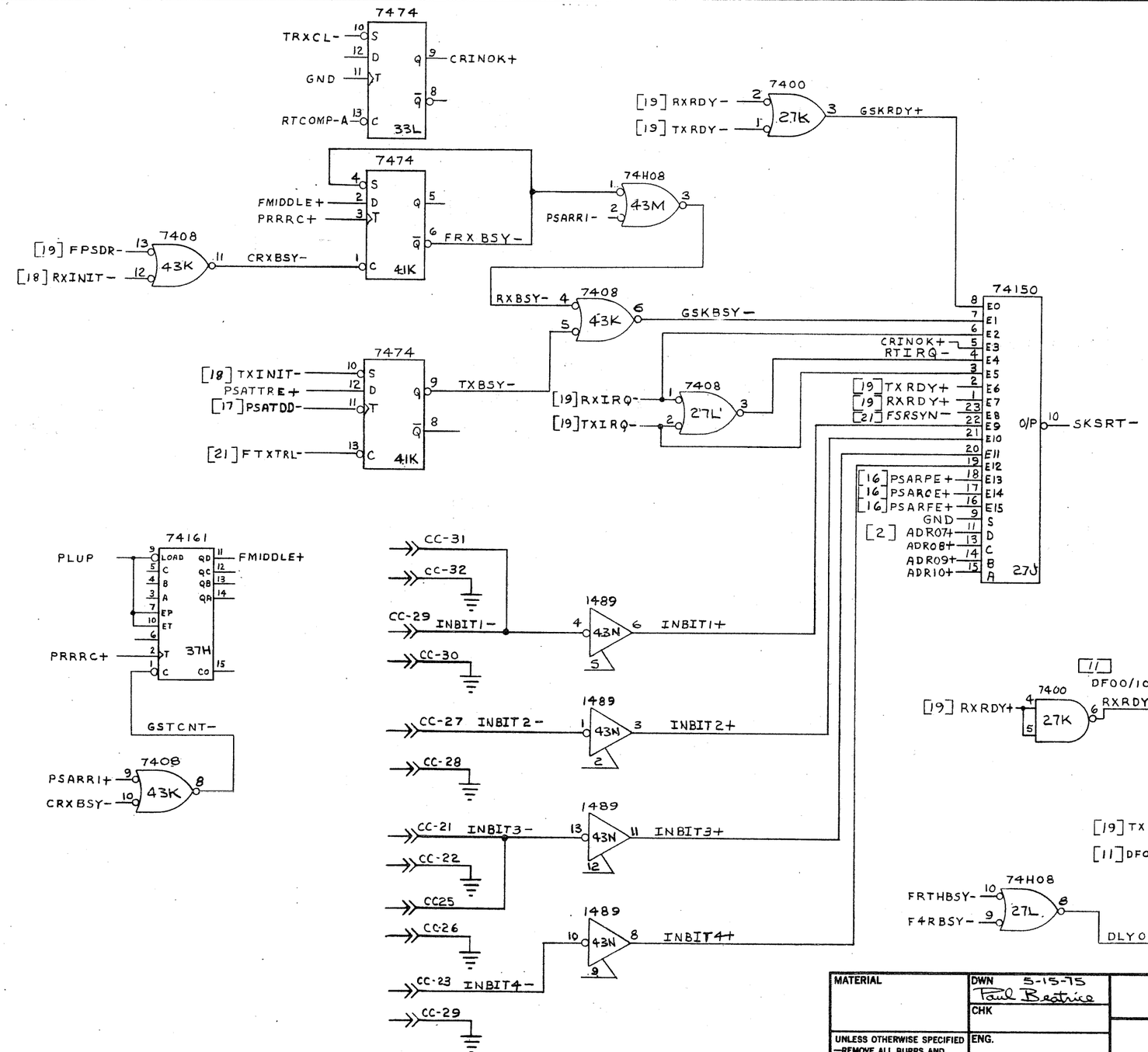


IV-20

MATERIAL	DWN Paul Beatrice 5-15-75	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC RX, TX } READY, IRQ, DRQ	
	ENG.		
	APPRD		
	USED ON	SCALE —	SIZE C
	NEXT ASSY	SHEET 19 OF	DWG. NO. LBD 2282 REV. A

PDF-003

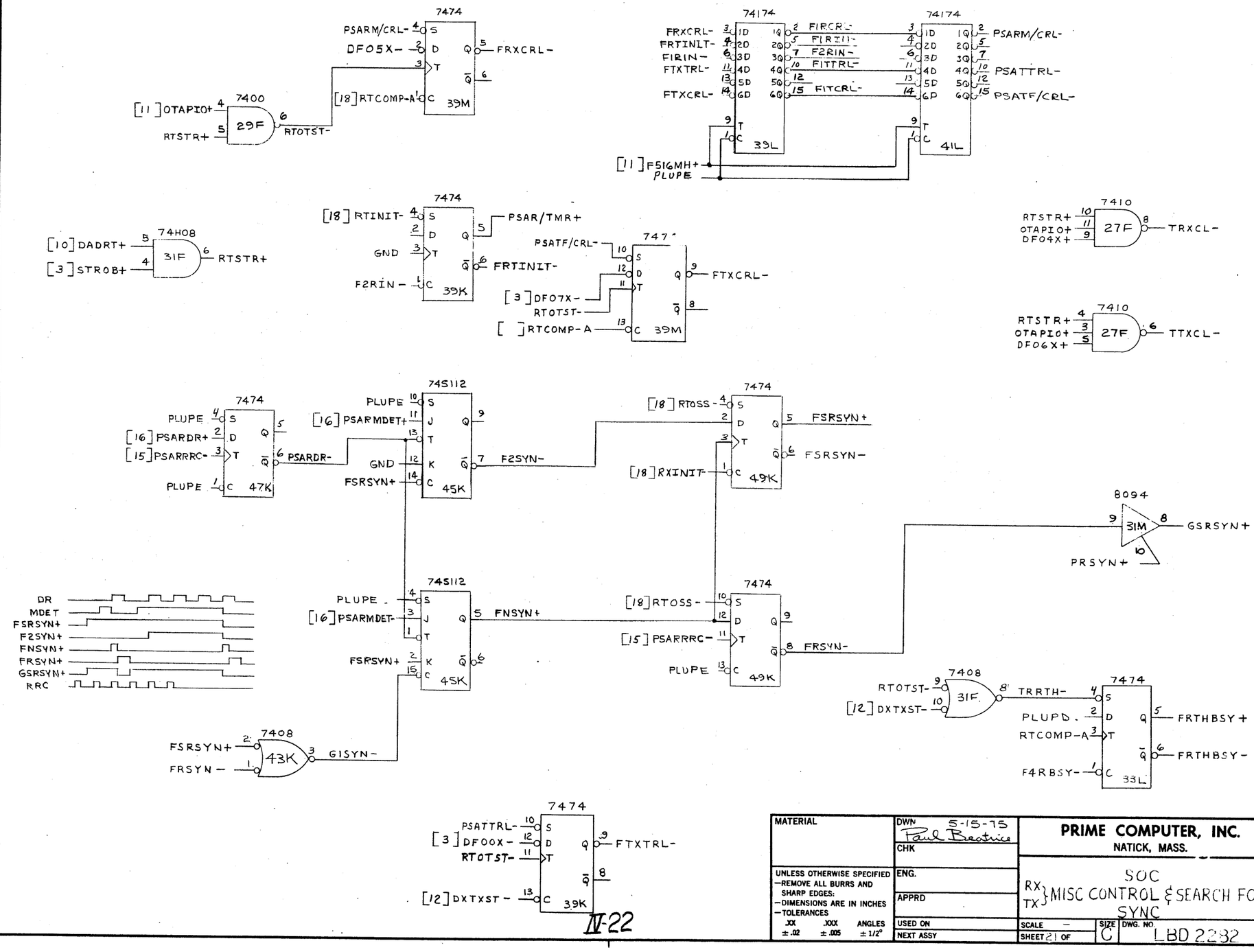
PRIME COMPUTER, INC.



IV-21

MATERIAL	DWN 5-15-75 Paul Bestrice	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	SOC RX/TX READY LOGIC
	ENG.	
	APPRD	
	USED ON	
	NEXT ASSY	SCALE — SHEET 20 OF — SIZE C — DWG. NO LBD 2282 — REV. A

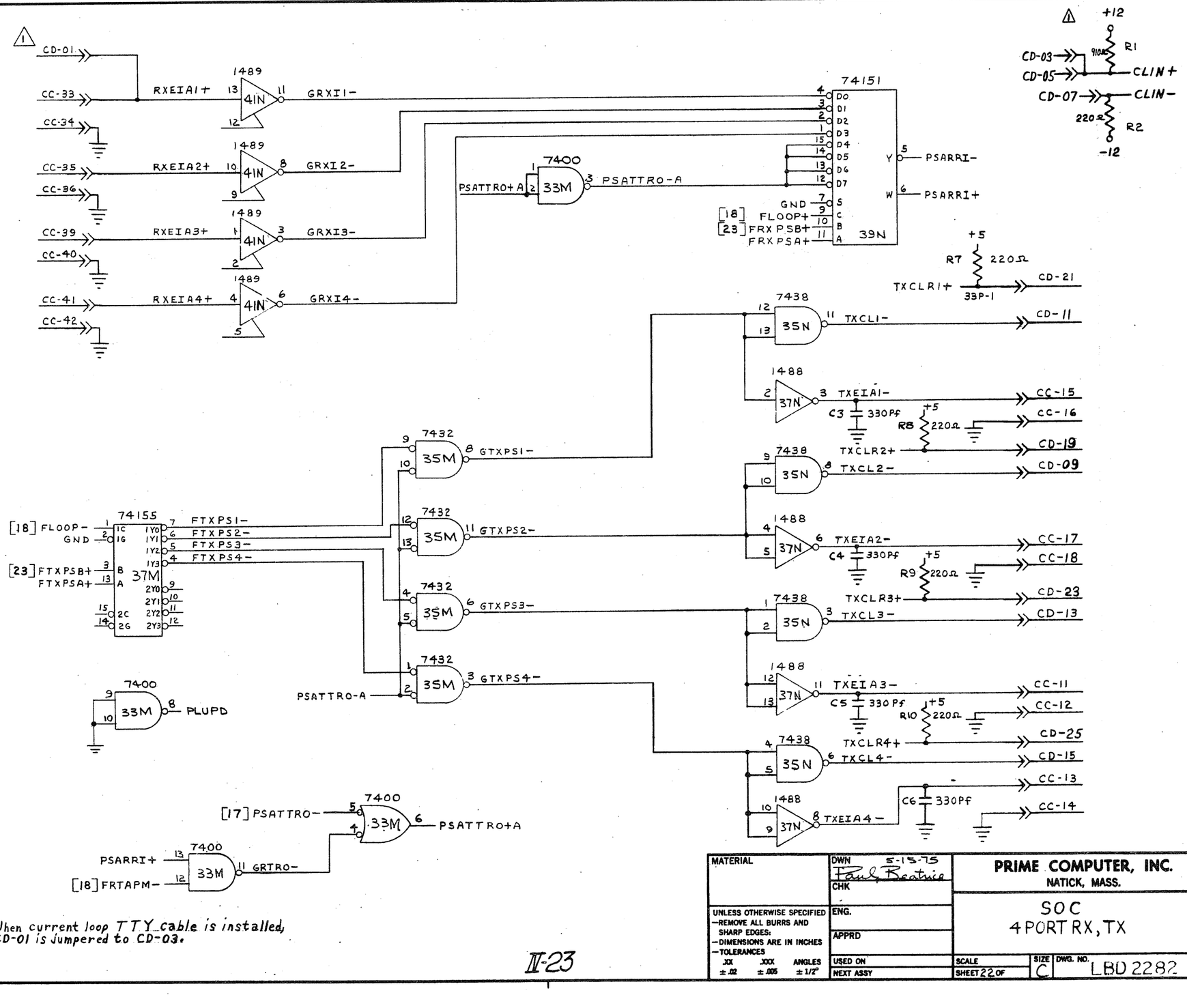
PDF-003



N-22

MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC RX/TX MISC CONTROL & SEARCH FOR SYNC	
	APPRD		
USED ON		SCALE —	SIZE C
NEXT ASSY		SHEET 21 OF	DWG. NO. LBD 2232 REV. A

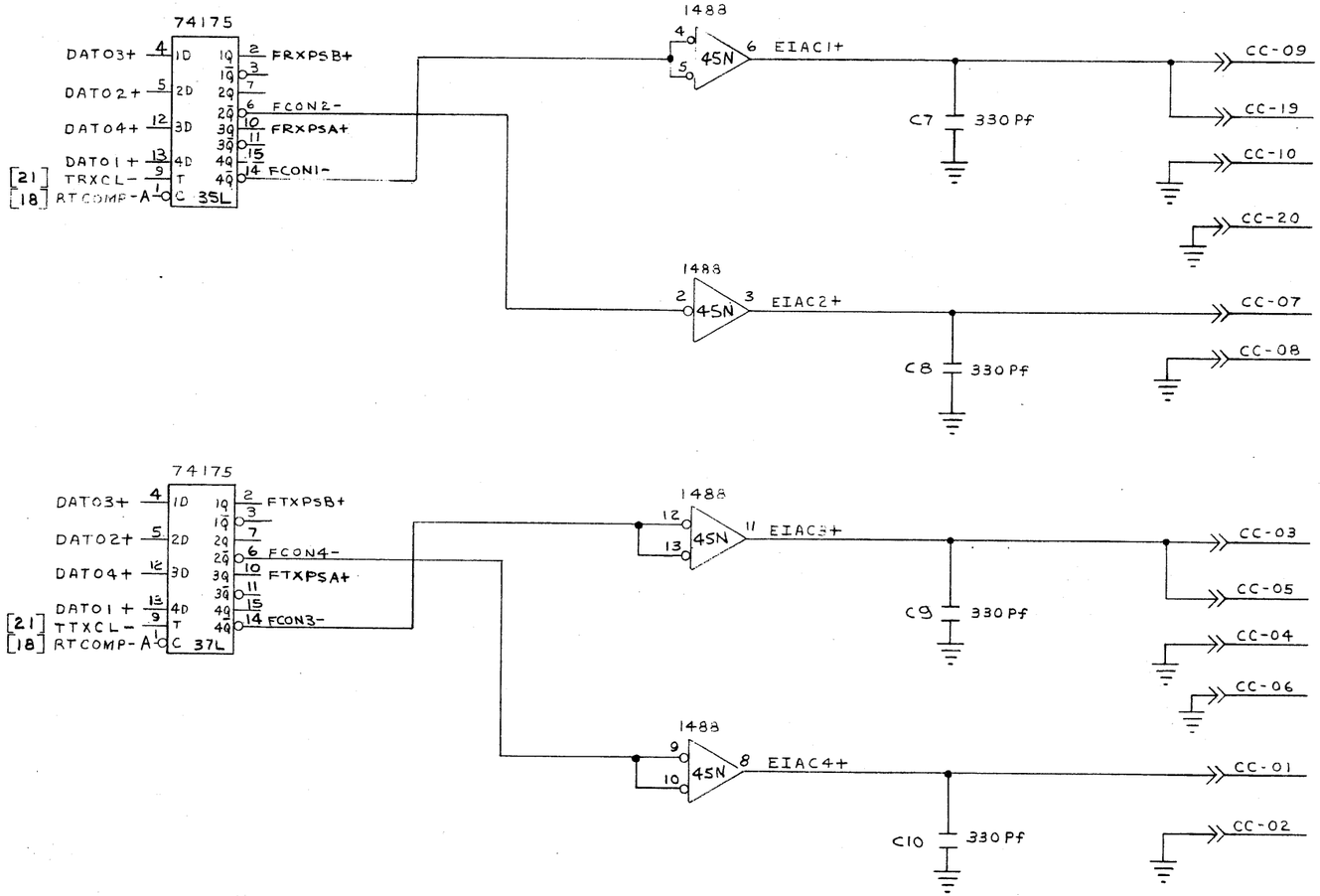
PDF-003



⚠1 When current loop TTY cable is installed, CD-01 is jumpered to CD-03.

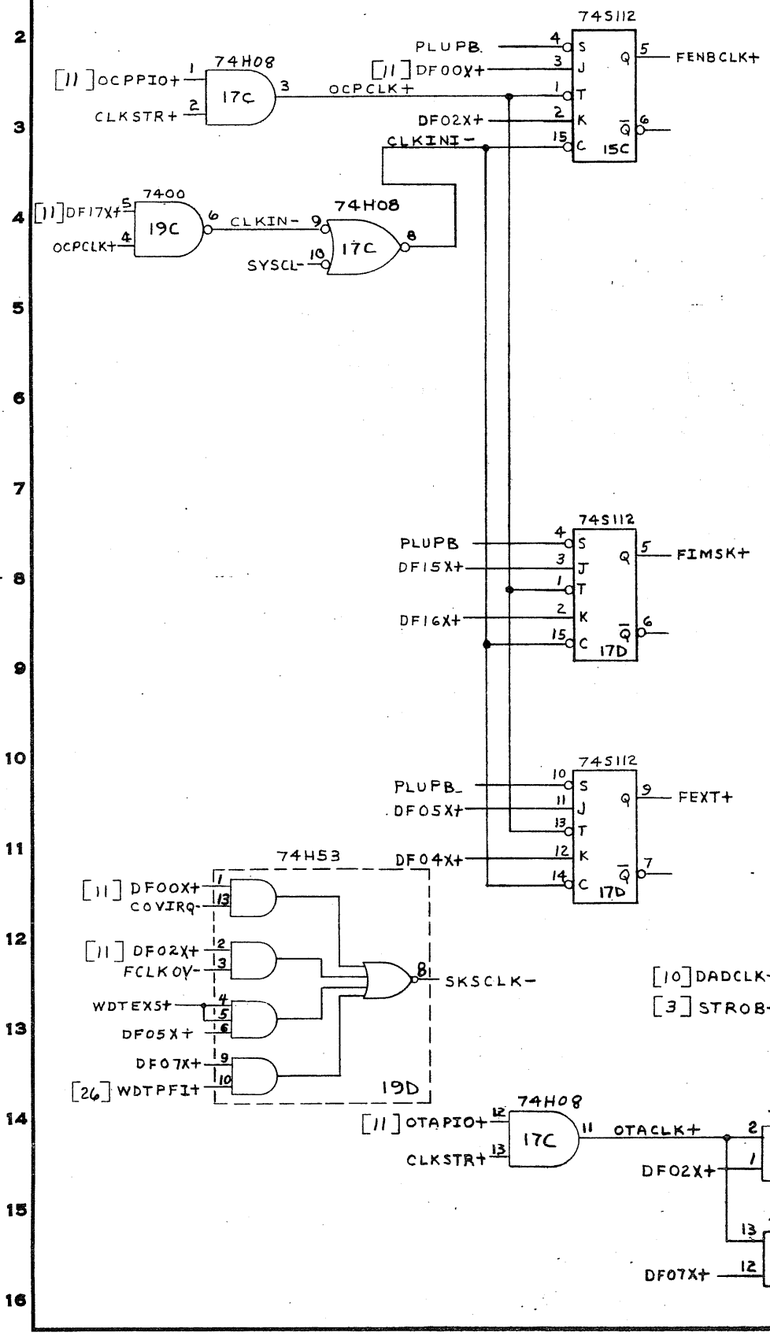
MATERIAL	DWN 5-13-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC 4 PORT RX, TX	
	ENG.		
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 22 OF	SIZE C / DWG. NO. LBD 2282 / REV. A

PDF-003



MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC CONBITS 1-4	
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 23 OF	SIZE C / DWG. NO. LBD 2232 / REV. A

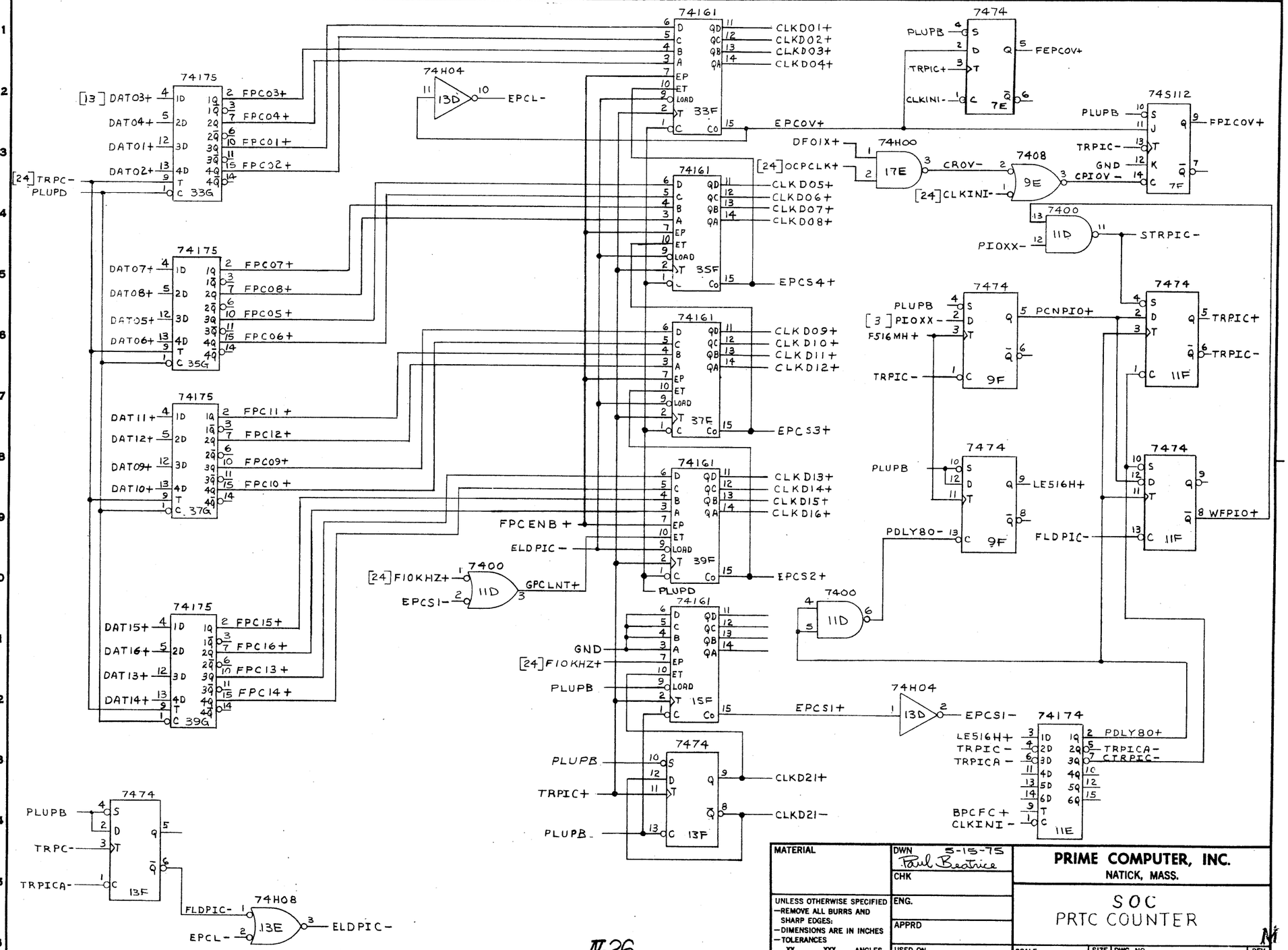
PDF-003



IV-25

MATERIAL	DWN Paul Beatrice 5-15-75	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC RTC CONTROL LOGIC
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 24 OF
		SIZE C / DWG. NO. LBD 2282 / REV. A

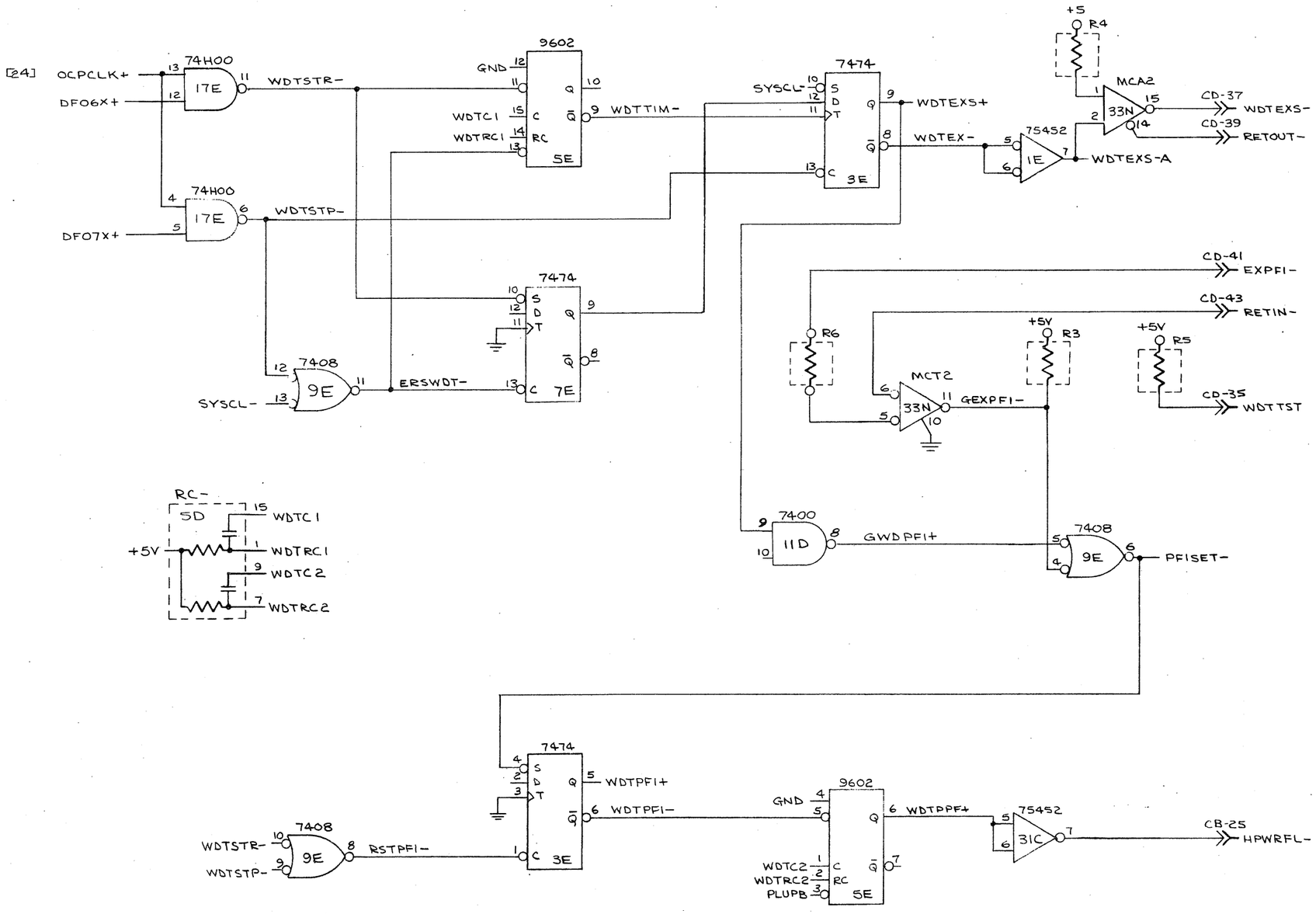
PDF-003



MATERIAL	DWN Paul Beatrice 5-15-75	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	SOC PRTC COUNTER	
	ENG.		
	APPRD		
USED ON / NEXT ASSY	SCALE	SIZE C	DWG. NO. LBD 2282 REV. A
	SHEET 25 OF		

PDF-003

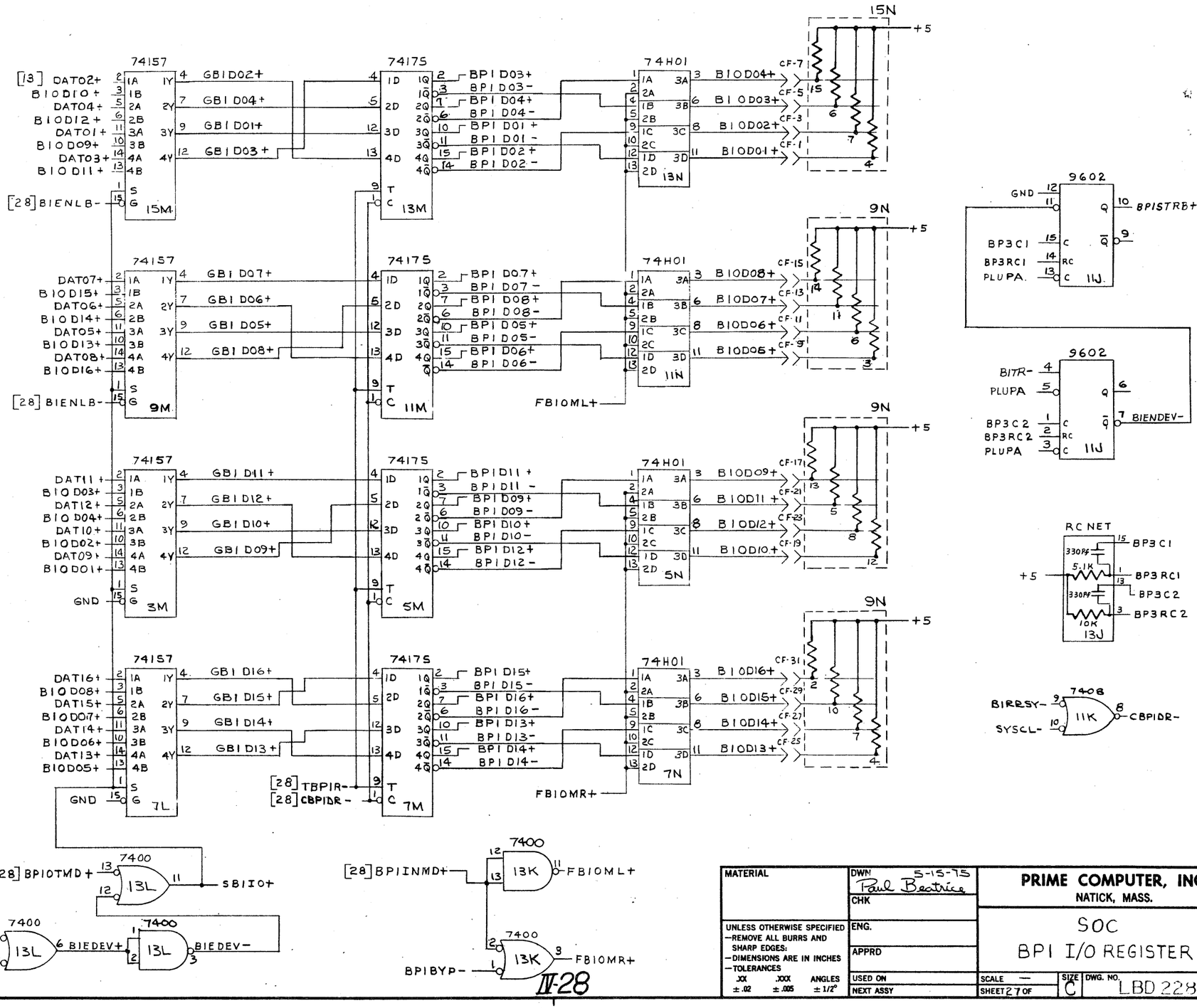
PRIME COMPUTER, INC.



MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	WATCH DOG TIMER SOC
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 26 OF / SIZE / DWG. NO. LBD 2282 / REV. A

PDF-003

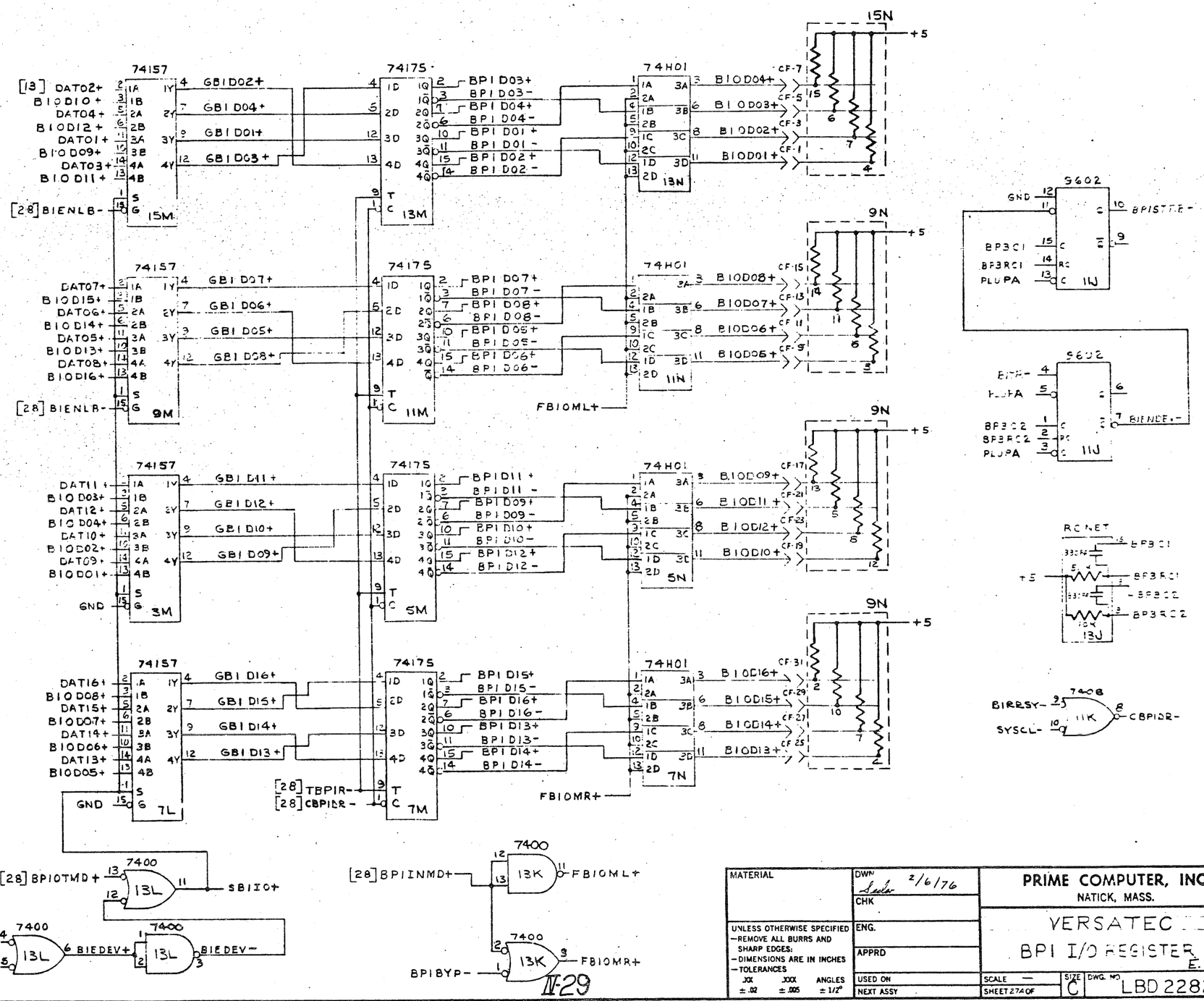
PRIME COMPUTER, INC.



MATERIAL	DWN Paul Beatrice 5-15-75	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC BP1 I/O REGISTER	
	APPRD		
	USED ON / NEXT ASSY	SCALE — / SHEET 27 OF	SIZE C / DWG. NO. LBD 2282 / REV A

PDF-003

PRIME COMPUTER, INC.



MATERIAL	DWN Seder 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	VERSATEC	
	APPRD	BPI I/O REGISTER E.V	
	USED ON / NEXT ASSY	SCALE — SHEET 27 OF	SIZE C DWG. NO LBD 2282 REV 1

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74157 15M
[18] DAT02+
BIODI0+
DAT04+
BIODI2+
DAT01+
BIODI9+
DAT03+
BIODI1+
[28] BIENLB-
GBIDO2+
GBIDO4+
GBIDO1+
GBIDO3+

74175 13M
BPIDO3+
BPIDO3-
BPIDO4+
BPIDO4-
BPIDO1+
BPIDO1-
BPIDO2+
BPIDO2-

74H01 13N
DBO4 BIODO4+
DBO3 BIODO3+
DBO2 BIODO2+
DBO1 BIODO1+

74157 9M
DAT07+
BIODI5+
DAT06+
BIODI4+
DAT05+
BIODI3+
DAT08+
BIODI6+
[28] BIENLB-
GBIDO7+
GBIDO6+
GBIDO5+
GBIDO8+

74175 11M
BPIDO7+
BPIDO7-
BPIDO8+
BPIDO8-
BPIDO5+
BPIDO5-
BPIDO6+
BPIDO6-

74H01 11N
DBO8 BIODO8+
DBO7 BIODO7+
DBO6 BIODO6+
DBO5 BIODO5+
FBIOML+

74157 3M
DATI1+
BIODO3+
DATI2+
BIODO4+
DATI0+
BIODO2-
DATO3-
BIODO1+
GND
GBIDI1+
GBIDI2+
GBIDI0+
GBIDI0+

74175 5M
BPIDI1+
BPIDI1-
BPIDI0+
BPIDI0-
BPIDI2+
BPIDI2-

74H01 5N
BIODO9+
BIODI1+
BIODI2+
BIODI3+

74157 7L
DATI6+
BIODO6+
DATI5+
BIODI7+
DATI4+
BIODO6+
DATI3+
BIODO5+
GND
GBIDI6+
GBIDI5+
GBIDI4+
GBIDI3+

74175 7M
[28] TBPIR-
[28] CBPIDR-
BPIDI5+
BPIDI5-
BPIDI6+
BPIDI6-
BPIDI3+
BPIDI3-
BPIDI4+
BPIDI4-

74H01 7N
FBIOMR+
BIODI6+
BIODI5+
BIODI4+
BIODI3+

15N +5
9N +5
9N +5
9N +5

9602 11J
GND
BPI3C1
BPI3RC1
PLUPA
BPISTRB+

9602 11J
BPI3C2
BPI3RC2
PLUPA
BIENDEV-

RC NET 13J
BPI3C1
+5
BPI3RC1
BPI3C2
BPI3RC2
330PF
10K

7408 11K
BIRRSY-
SYSCL-
CBPIDR-

7400 13L
[28] BPIOTMD+
SBIICI+

7400 13L
BIENDEV-
[28] BITRDY-
BIEDEV+
BIEDEV-

7400 13K
[28] BPIINMD+
FBIOML+

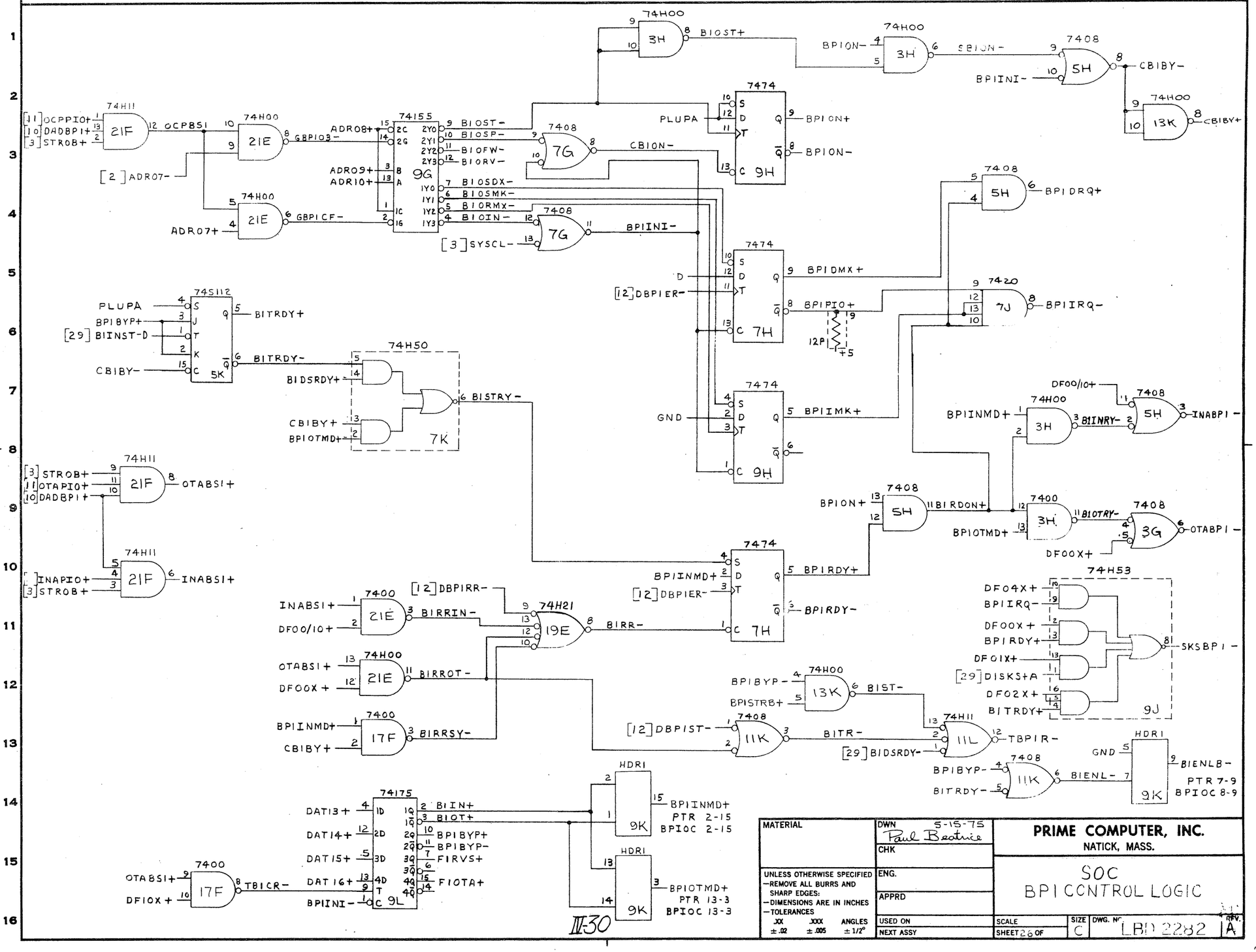
7400 13K
BPIBYP-
FBIOMR+

II-29A

MATERIAL	DWN Leslie 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	GOULD	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	BPI I/O REGISTER	
	APPRD	E.V M	
	USED ON / NEXT ASSY	SCALE — / SHEET 27B-F	SIZE C / DWG. NO LBD 2282 / REV 1

PDF-003

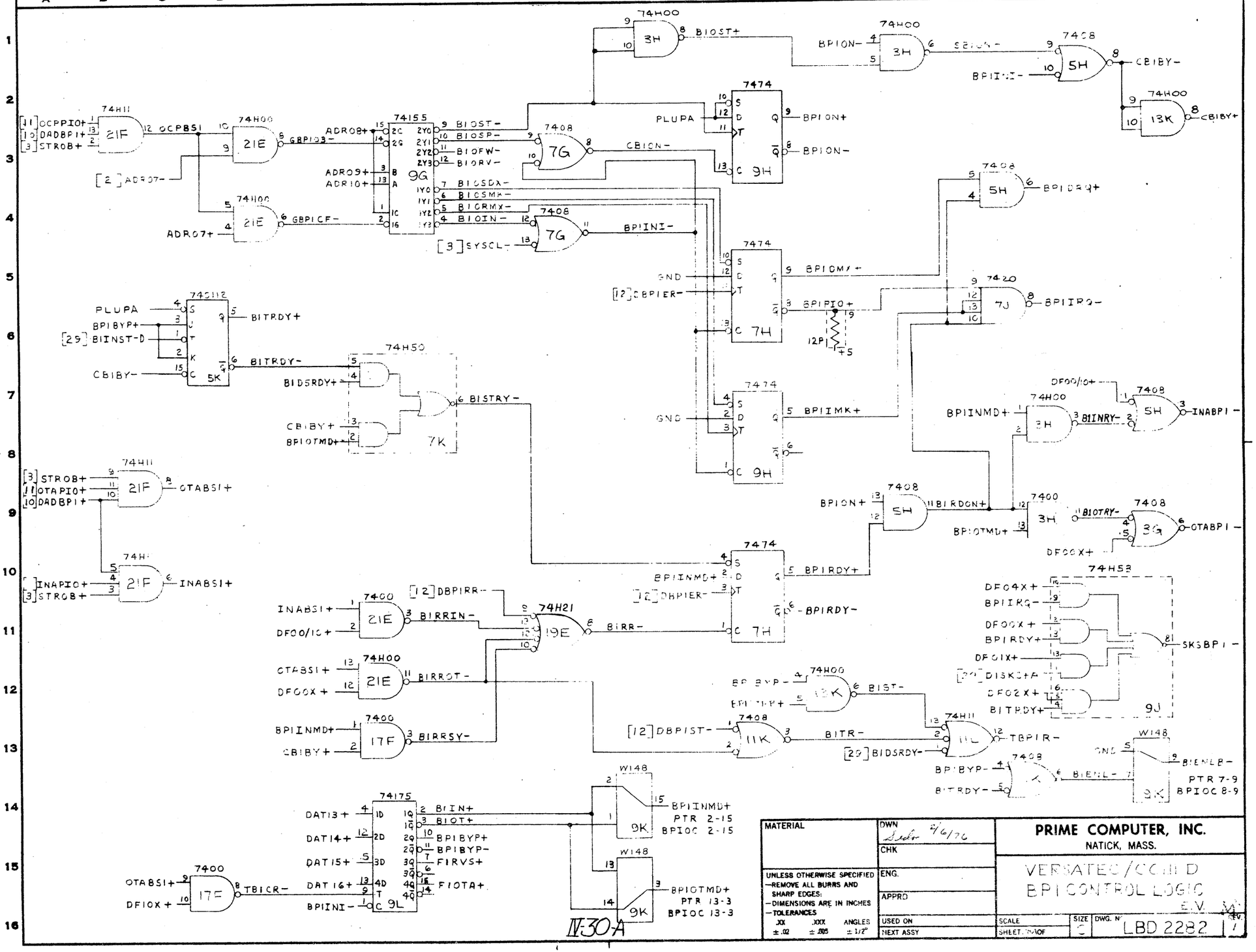
PRIME COMPUTER, INC.



MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC BPI CONTROL LOGIC	
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 26 OF	SIZE C / DWG. NO. LBD 2282 / REV. A

PDF-003

PRIME COMPUTER, INC.

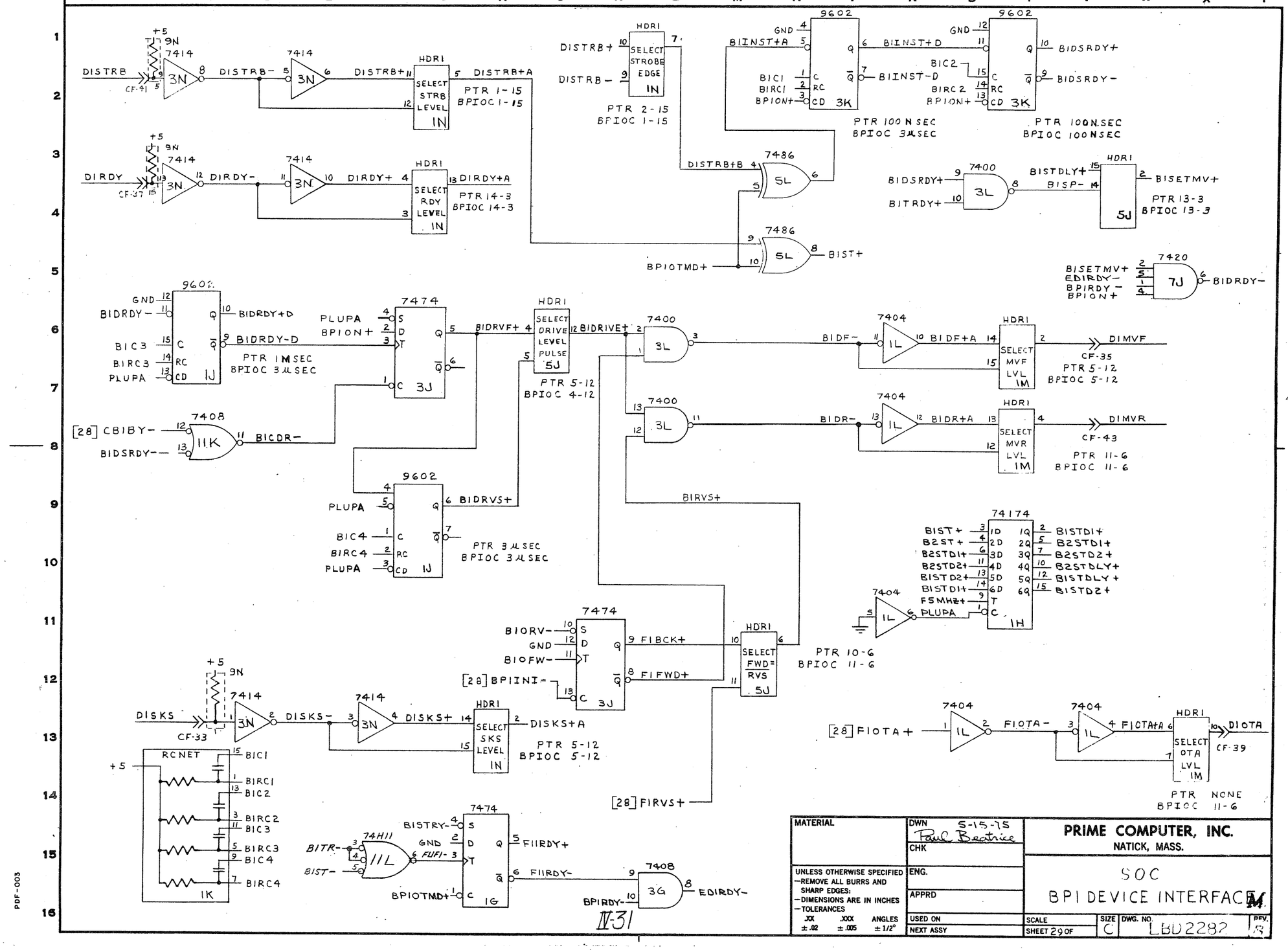


II-30-A

MATERIAL	DWN Leder 9/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	VERSATEC/CCHD BPI CONTROL LOGIC	
	APPRO	E.V.	
	USED ON	SCALE	SIZE C DWG. NO LBD 2282 REV M
	NEXT ASSY	SHEET 1 OF	1

PDF-003

PRIME COMPUTER, INC.



MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC BPI DEVICE INTERFACE	
	APPRD		
	USED ON	SCALE	SIZE C
	NEXT ASSY	SHEET 29 OF	DWG. NO. LBD2282 REV. R

PDF-003

IV-31

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

READY DISTRB — CF-41 — +5 9N — 7414 3N — DISTRB− — 7414 3N — DISTRB+ — W152 SELECT STRB LEVEL IN — DISTRB+A — PTR 1-15 BPIOC 1-15

READY DIRDY — CF-37 — +5 9N — 7414 3N — DIRDY− — 7414 3N — DIRDY+ — W152 SELECT RDY LEVEL IN — DIRDY+A — PTR 4-3 BPIOC 14-3

DISTRB+ / DISTRB− — W152 SELECT STROBE EDGE IN — PTR 2-15 BPIOC 1-15

BINST+A — 9602 — BINST+D — BINST−D — PTR 100 NSEC BPIOC 3 μSEC

BIC2 / BIRC2 / BPION+ — 9602 — BIDSRDY+ / BIDSRDY− — PTR 100NSEC BPIOC 100NSEC

DISTRB+B — 7486 5L

BIDSRDY+ / BITRDY+ — 7400 3L — BISTDLY+ — W154 SELECT BISP LEVEL 5J — BISETMV+ — PTR 13-3 BPIOC 13-3

BPIOTMD+ — 7486 5L — BIST+

BISETMV+ / EDIRDY− / BPIRDY− / BPION+ — 7420 7J — BIDRDY−

BIDRDY− / BIC3 / BIRC3 / PLUPA — 9602 — BIDRDY+D / BIDRDY−D — PTR 1 MSEC BPIOC 3 μSEC

PLUPA / BPION+ — 7474 3J — BIDRVF+ — W154 SELECT DRIVE LEVEL PULSE 5J — BIDRIVE+ — PTR 5-12 BPIOC 4-12

7400 2L — BIDF− — 7404 1L — BIDF+A — W153 SELECT MVF LVL 1M — DIMVF — CF-35 PTR 5-12 BPIOC 5-12 — PICLK

7400 3L — BIDR− — 7404 1L — BIDR+A — W153 SELECT MVR LVL 1M — DIMVR — CF-43 PTR 11-6 BPIOC 11-6 — RLTER

[28] CBIBY− / BIDSRDY− — 7408 11K — BICDR−

9602 — PLUPA / BIC4 / BIRC4 / PLUPA — BIDRVS+ — PTR 3 μSEC BPIOC 3 μSEC

BIRVS+

74174 — BIST+ / B2ST+ / B2STD1+ / B2STD2+ / BIST D2+ / BIST D1+ / FSMHZ+ — 1Q–6Q — BISTD1+ / B2STD1+ / B2STD2+ / B2STDLY+ / BISTDLY+ / BISTD2+ — 7404 1L — PLUPA — 1H

7474 — BIORV− / GND / BIOFW− / [28] BPIINI− — FIBCK+ / FIFWD+ — W154 SELECT FWD= RVS 5J — PTR 10-6 BPIOC 11-6

[28] FIRVS+

ON LINE DISKS — CF-33 — +5 9N — 7414 3N — DISKS− — 7414 3N — DISKS+ — W152 SELECT SKS LEVEL IN — DISKS+A — PTR 5-12 BPIOC 5-12

RCNET — +5 — BIC1 / BIRC1 / BIC2 / BIRC2 / BIC3 / BIRC3 / BIC4 / BIRC4 — 1K

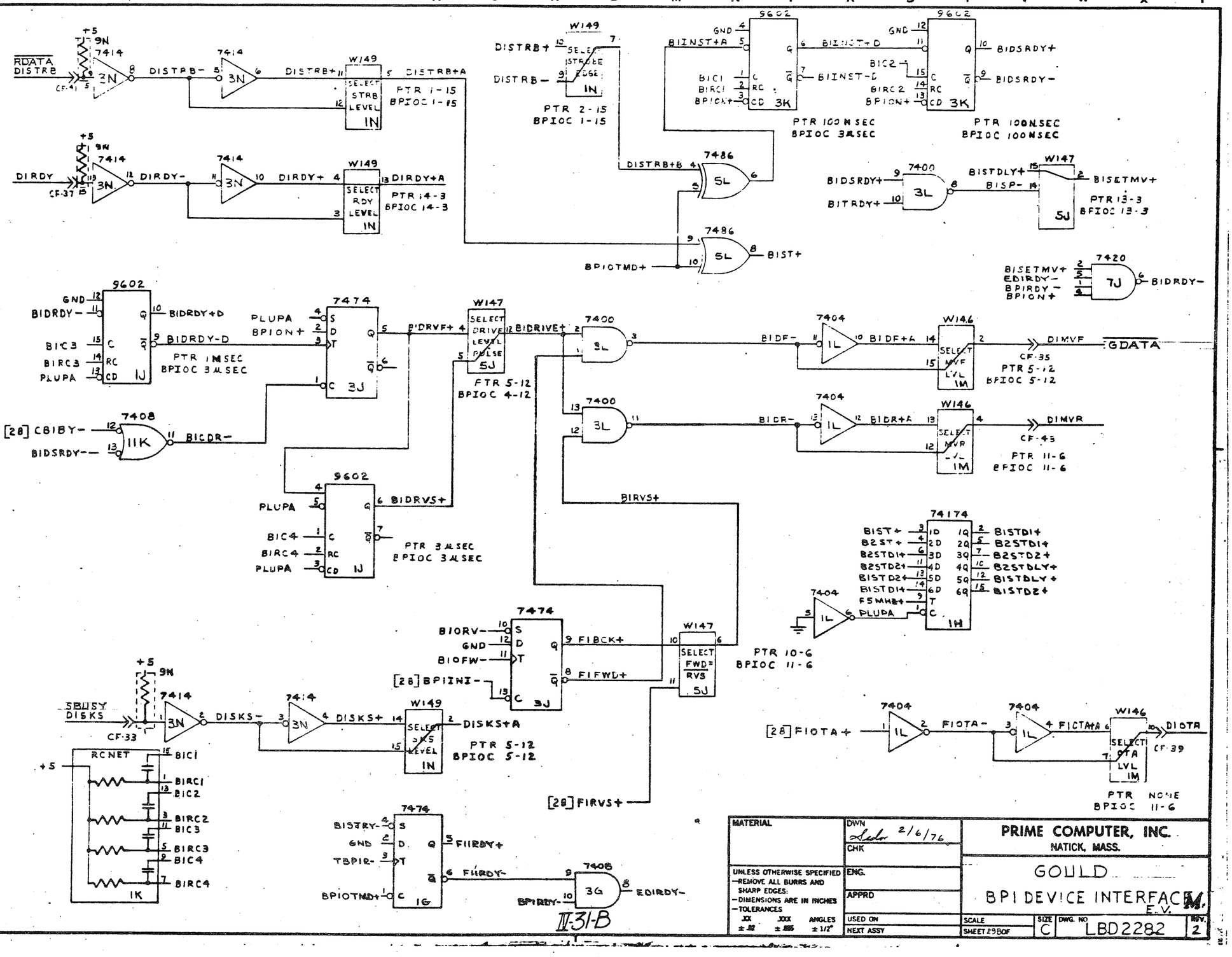
[28] FIOTA+ — 7404 1L — FIOTA− — 7404 1L — FIOTA+A — W153 SELECT OTA LVL 1M — DIOTA — CF-39 — PTR NONE BPIOC 11-6

7474 — BISTRY− / GND / TBPIR− / BPIOTMD+ — FIIRDY+ / FIIRDY− — 7408 3G — EDIRDY− / BPIRDY−

IV-31-A

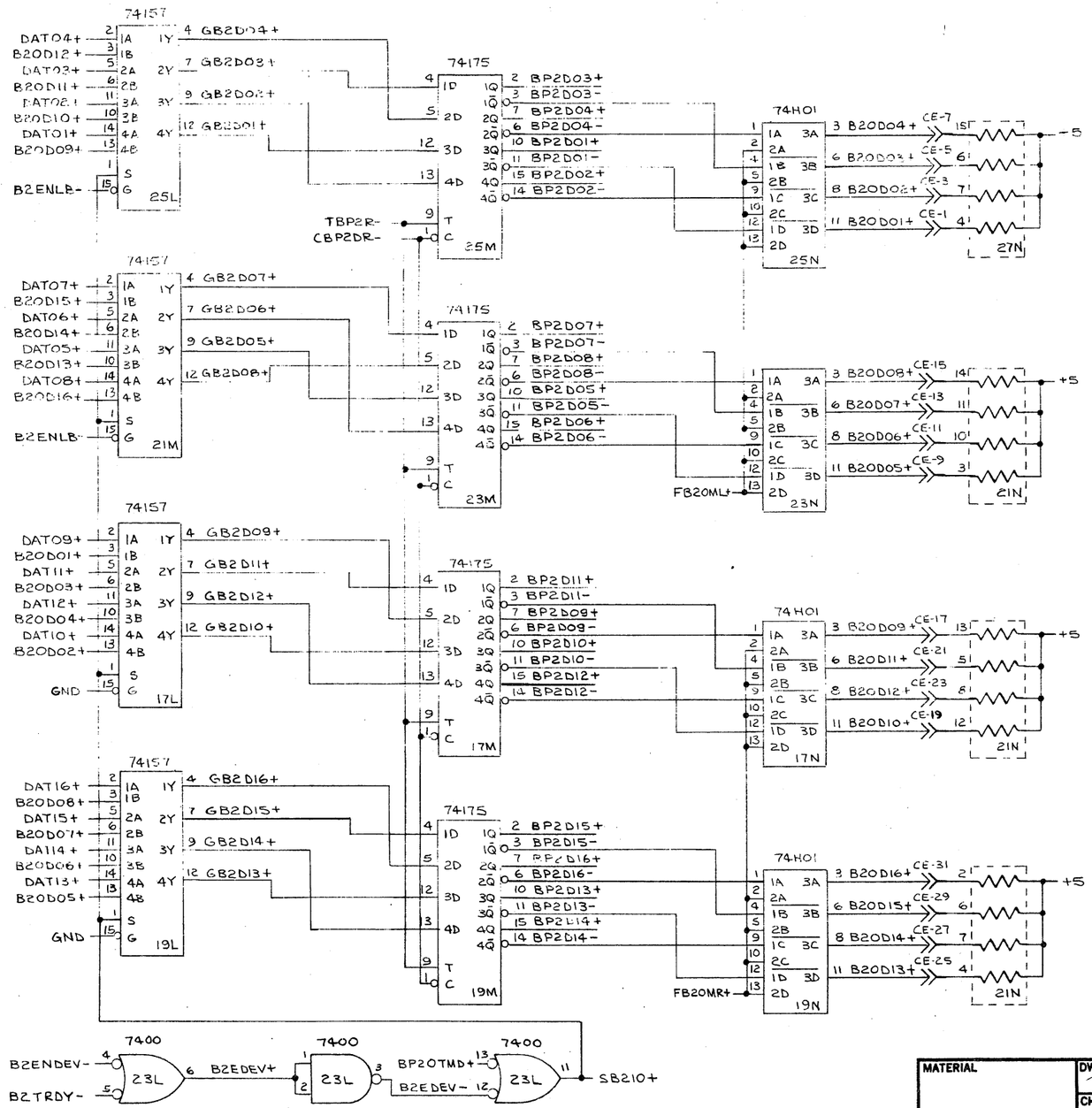
MATERIAL	DWN 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	VERSATEC BPI DEVICE INTERFACE E.V.	
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 29A OF	SIZE C / DWG. NO. LBD2282 / REV. 2

PRIME COMPUTER, INC.



II-31-B

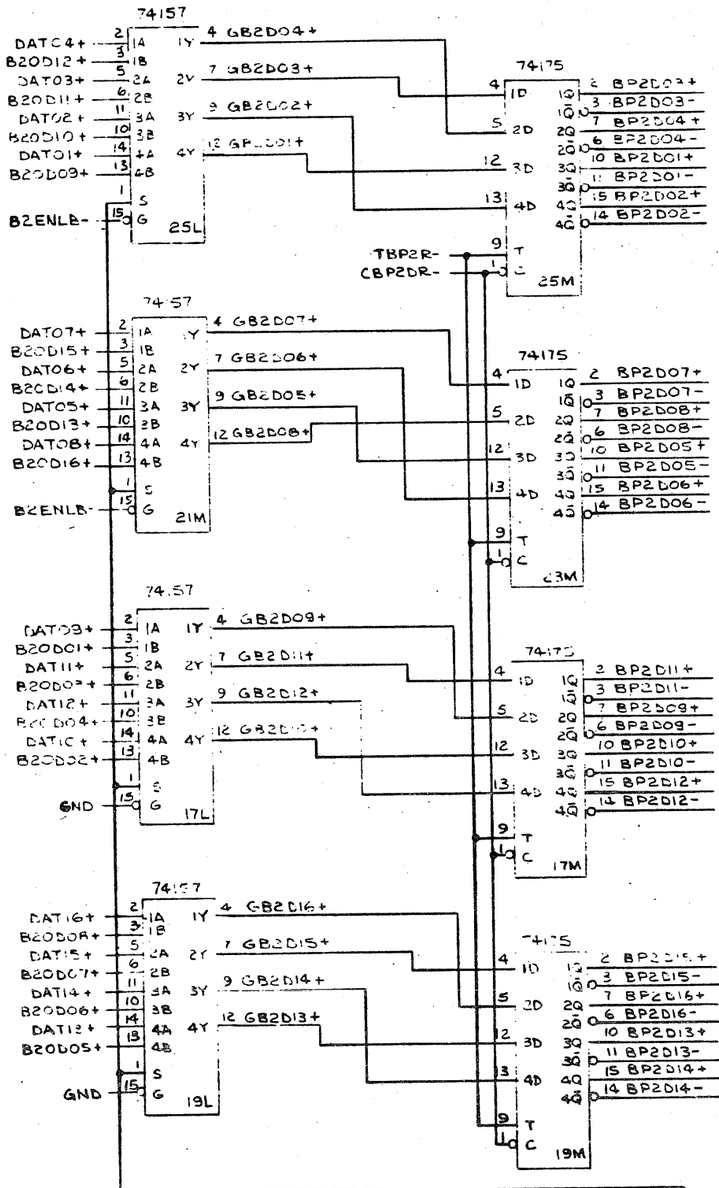
MATERIAL	DWN Lido 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	GOULD BPI DEVICE INTERFACE, E.V.	
	ENG.		
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 29 OF	SIZE C / DWG. NO LBD2282 / REV. 2



MATERIAL	DWN Paul Beatrice 5-15-75	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SOC BP2 I/O REGISTER	
	APPRD		
	USED ON / NEXT ASSY	SCALE —— SHEET 30 OF	SIZE C DWG. NO. LBD 2282 REV. A

PDF-003

PRIME COMPUTER, INC.

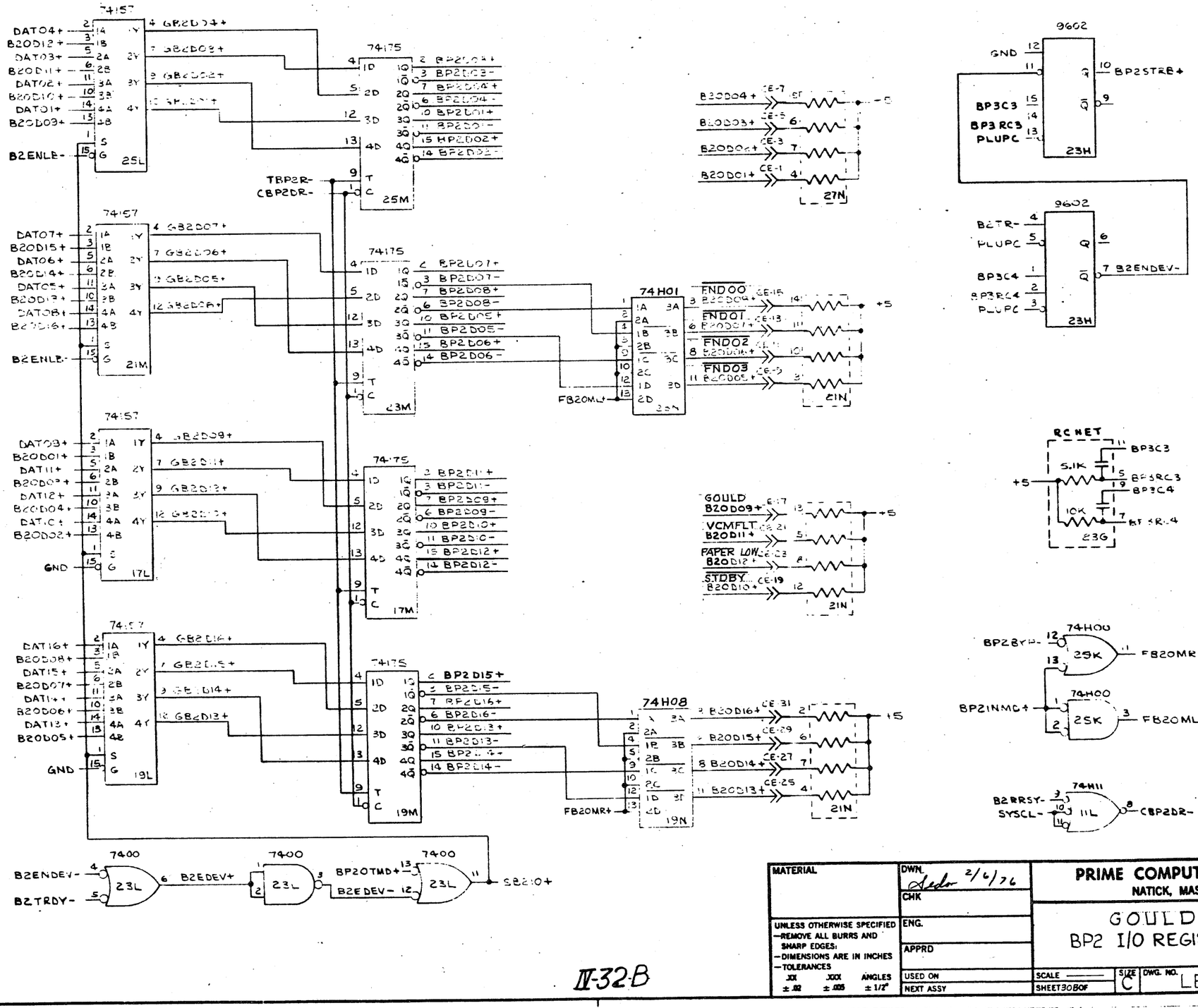


MATERIAL	DWN Leslo 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ± 1/2°	ENG.	VERSATEC BP2 I/O REGISTER E.V.	
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD 2282 REV. 1
	NEXT ASSY	SHEET 30A OF	

II-32-A

PDF-003

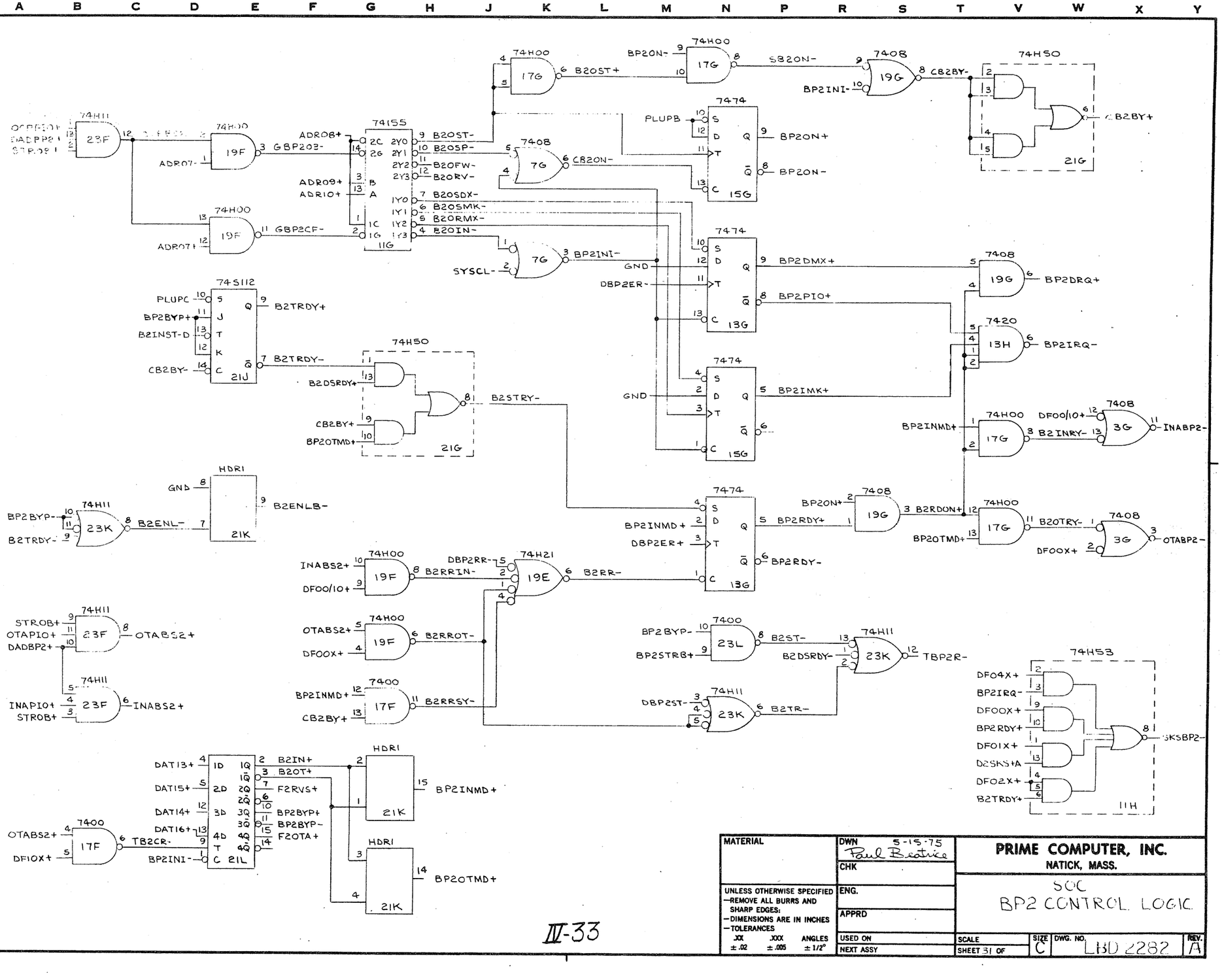
PRIME COMPUTER, INC.



II-32-B

MATERIAL	DWN Seder 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	GOULD BP2 I/O REGISTER E.V.
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE — SHEET 30 OF — SIZE C DWG. NO. LBD 2282 REV. 2

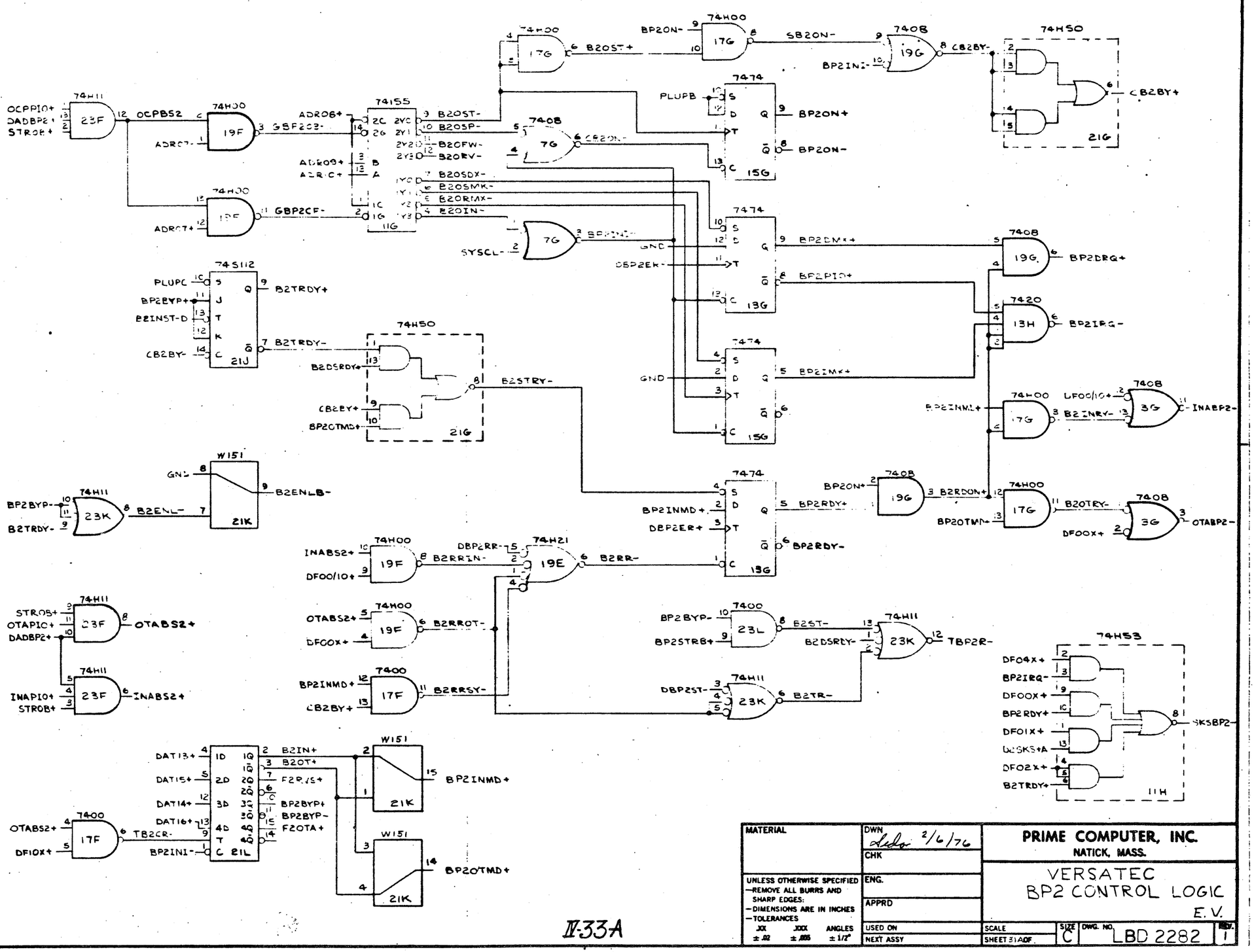
POF-003



MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	SOC BP2 CONTROL LOGIC	
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD 2282 REV. A
	NEXT ASSY	SHEET 31 OF	

PDF-003

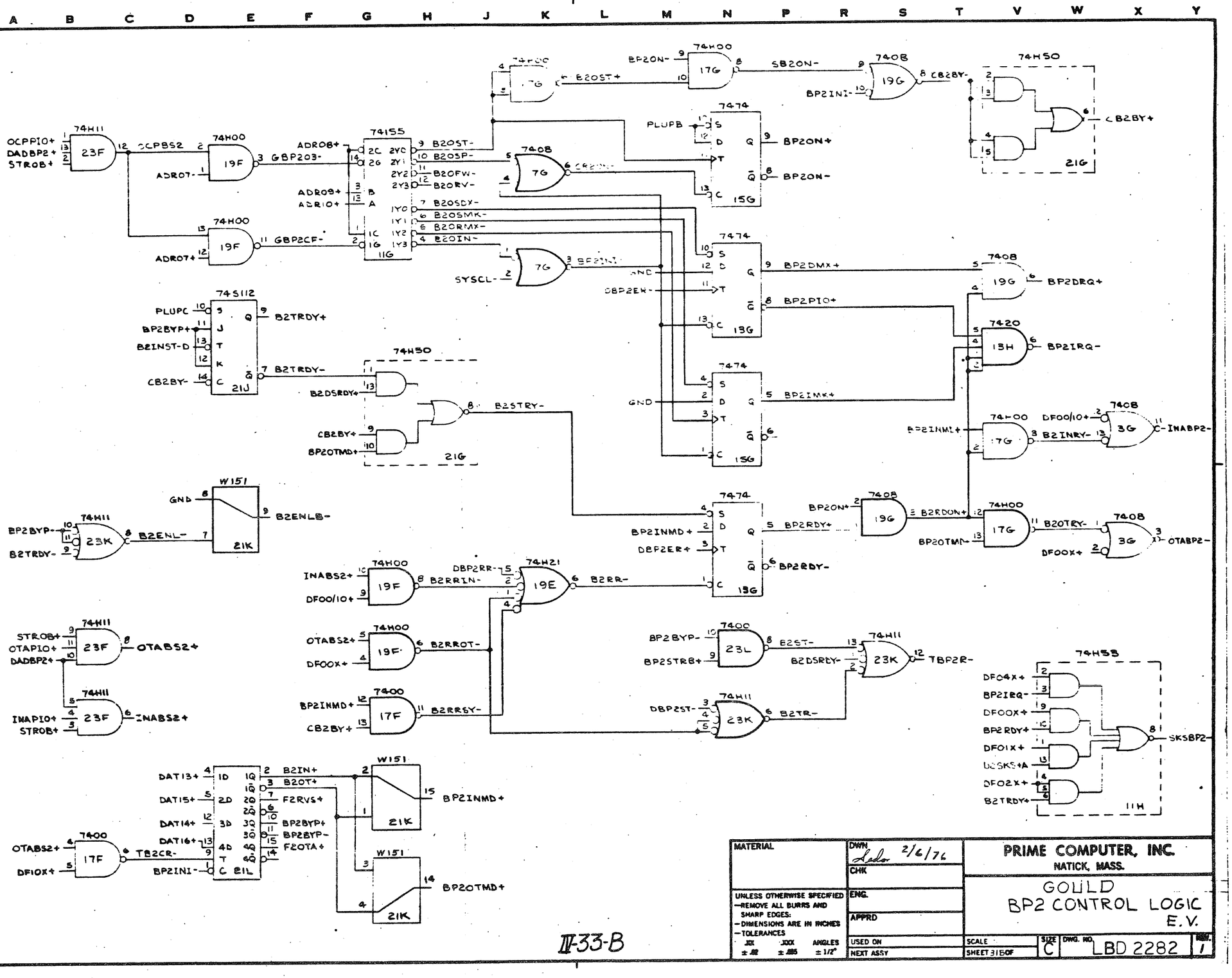
PRIME COMPUTER, INC.



II-33A

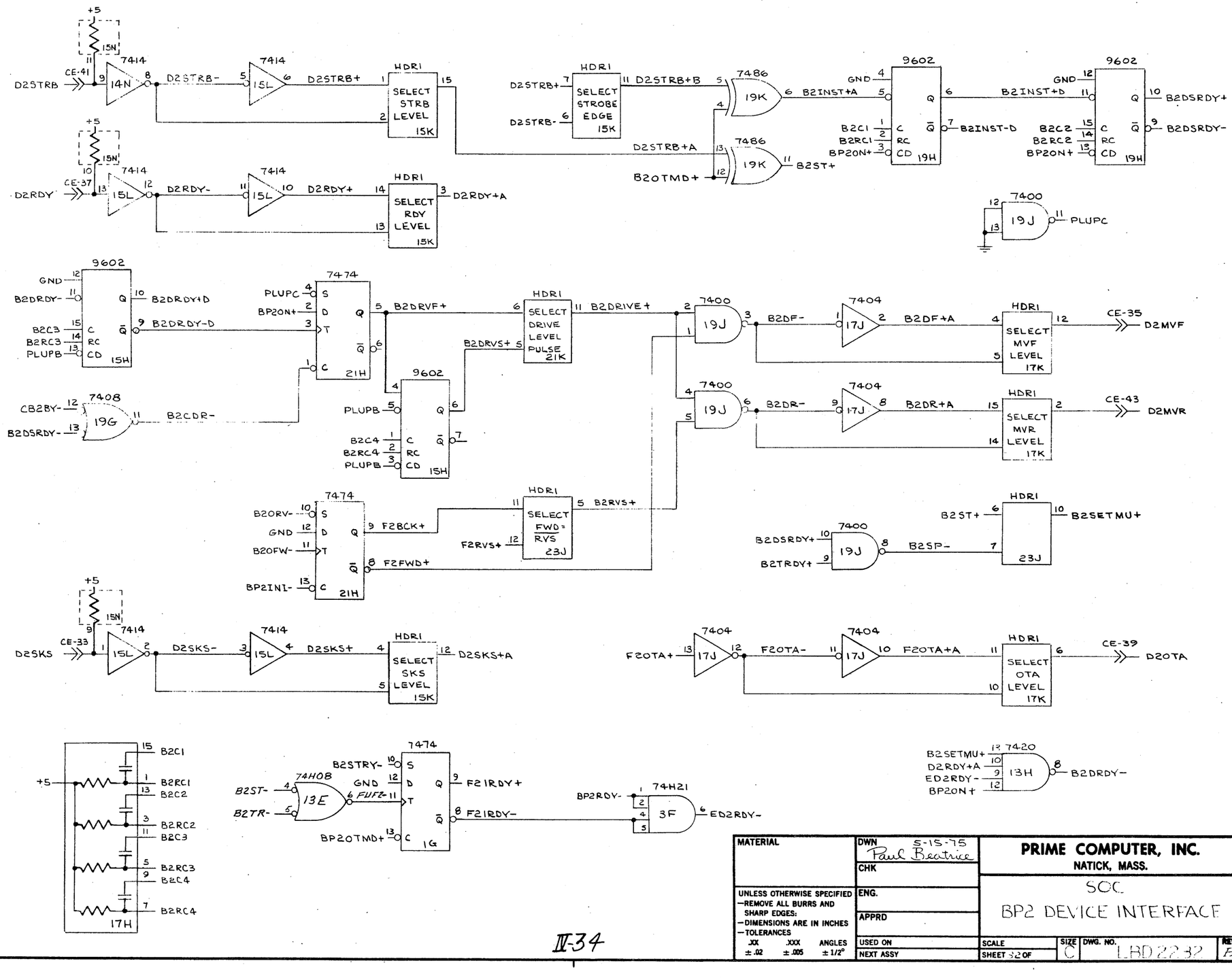
MATERIAL	DWN Lida 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	VERSATEC BP2 CONTROL LOGIC E.V.	
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD 2282 REV. 1
	NEXT ASSY	SHEET 31 OF	

PRIME COMPUTER, INC.



IV-33-B

MATERIAL	DWN Ledo 2/6/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	GOULD BP2 CONTROL LOGIC E.V.	
	APPRD		
	USED ON / NEXT ASSY	SCALE - / SHEET 31 OF	SIZE C / DWG. NO. LBD 2282 / REV. 1

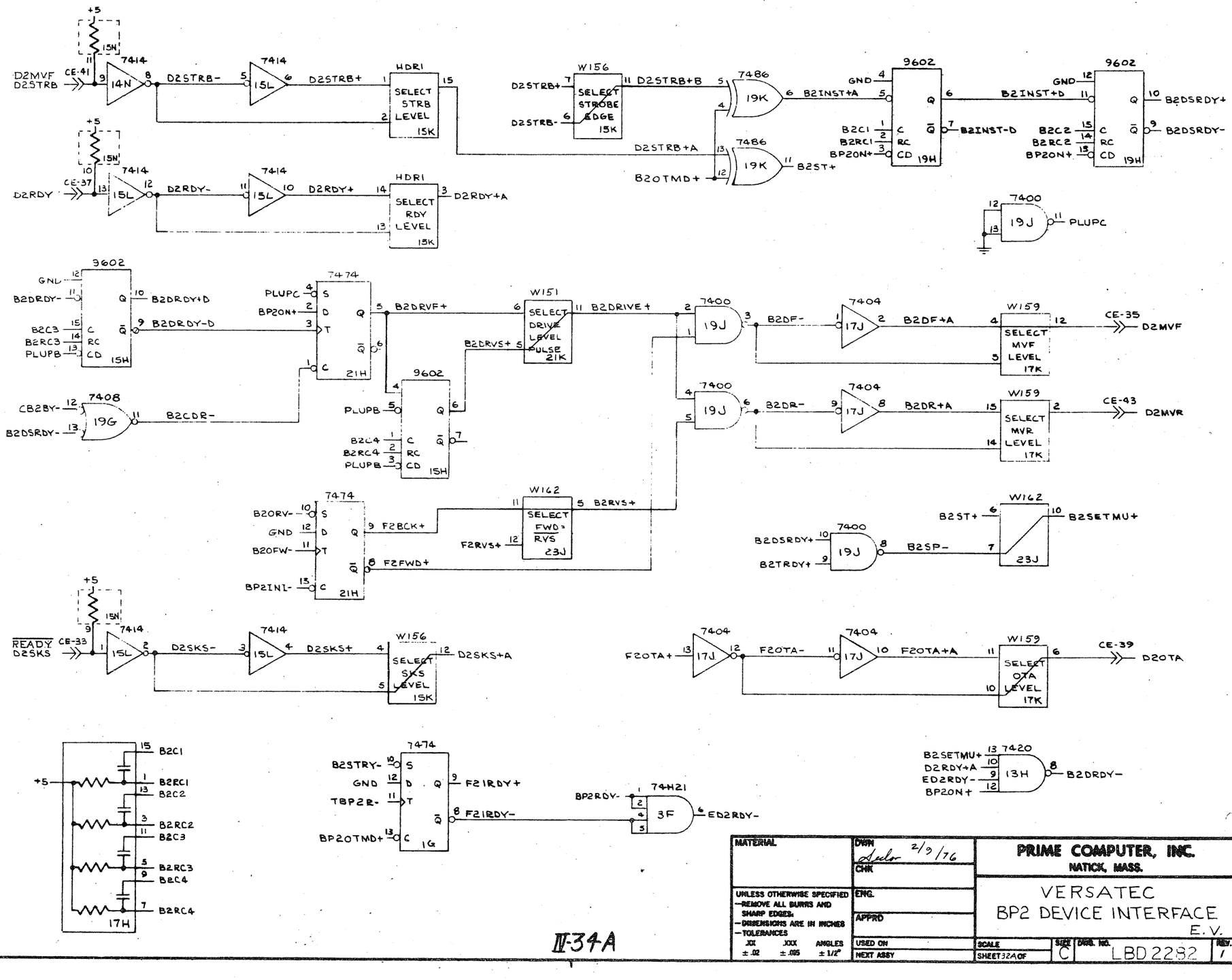


MATERIAL	DWN 5-15-75 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	SCC BP2 DEVICE INTERFACE	
	APPRD		
	USED ON	SCALE	SIZE C
	NEXT ASSY	SHEET 32 OF	DWG. NO. LBD2232 REV. B

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

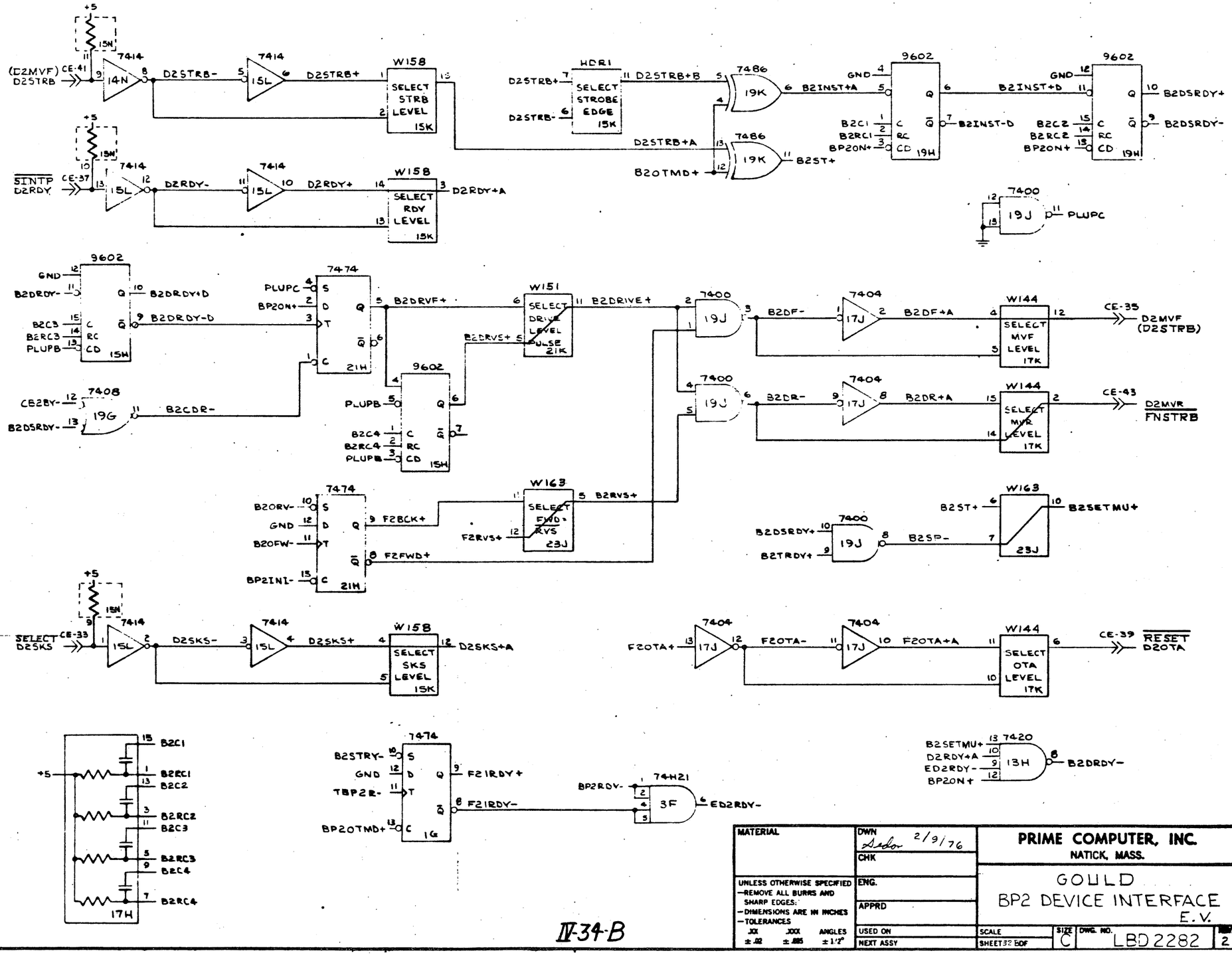
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16



MATERIAL	DWN Sulo 2/9/76	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	VERSATEC BP2 DEVICE INTERFACE E.V.
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 32A OF	SIZE C	DWG. NO. LBD2282	REV. 1

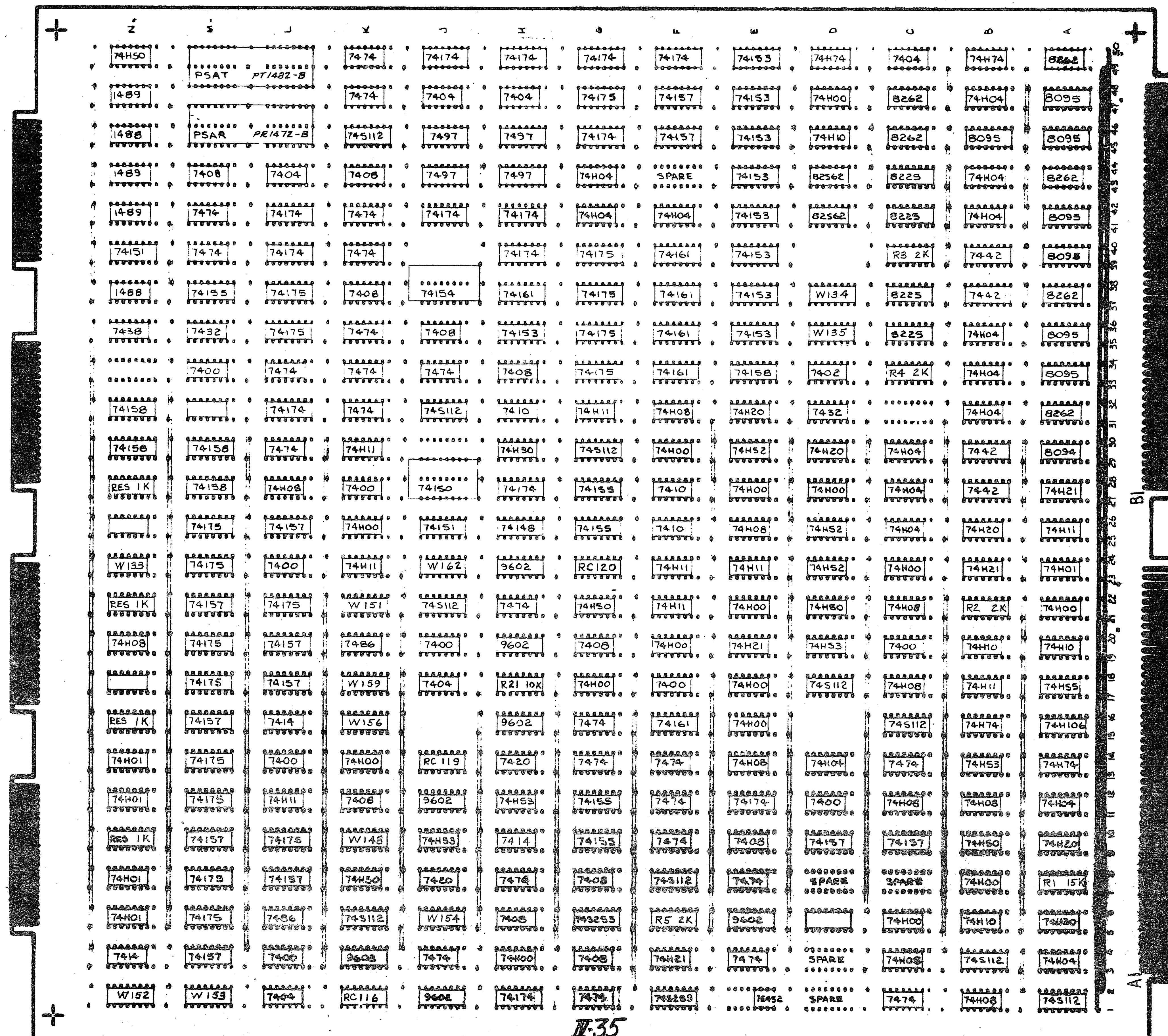
II-34A

PDF-003



IV-34-B

MATERIAL	DWN Sadon 2/9/76	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	GOULD BP2 DEVICE INTERFACE E.V.	
	ENG.		
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD2282 REV. 2
	NEXT ASSY	SHEET 32 EOF	

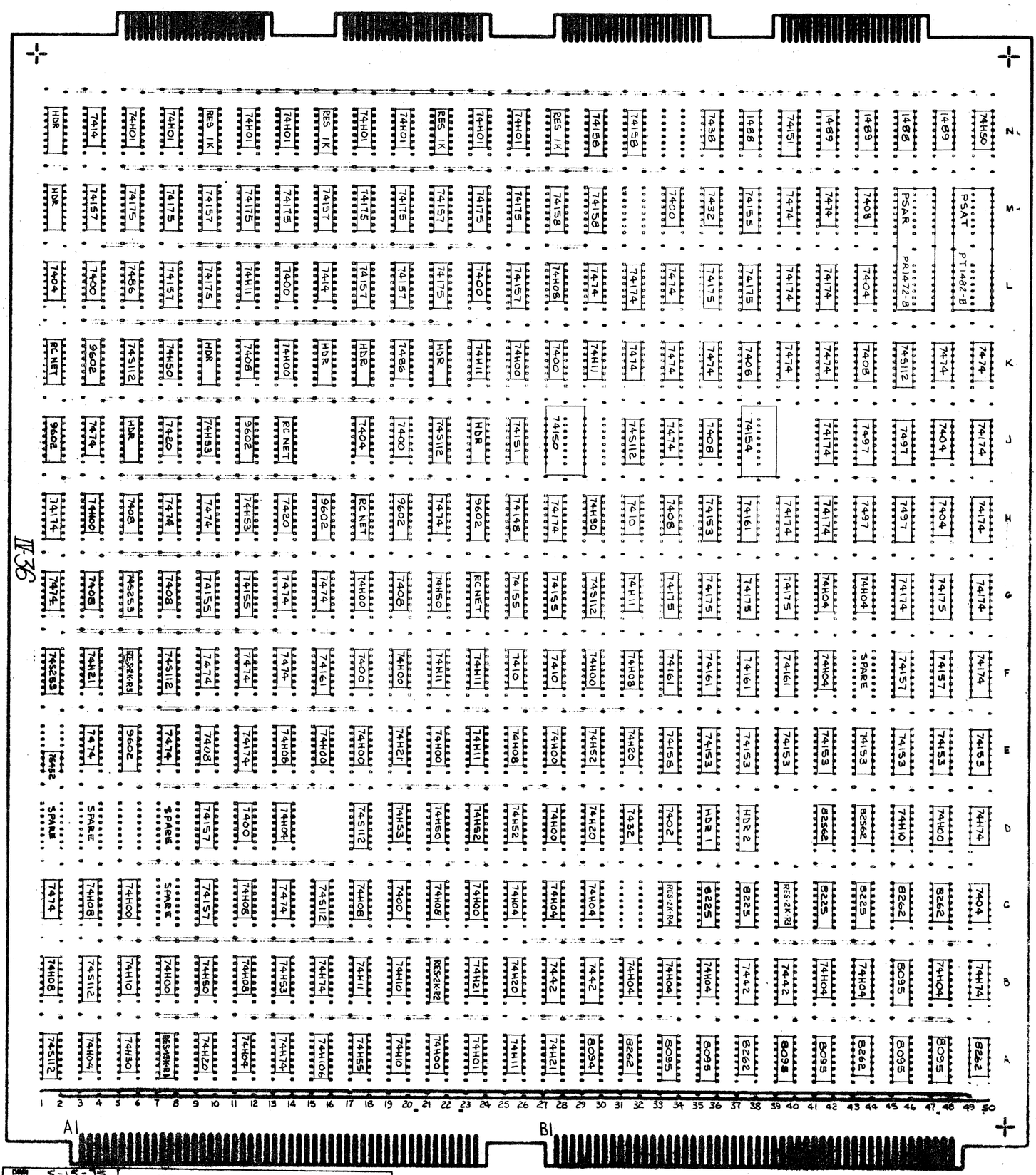


PRIME COMPUTER INC.
NATICK, MASS.

VERSATEC
DIP ALLOCATION

E.V.

C LBD 2282 1



DRN Paul Bastien 5-15-75	PRIME COMPUTER INC. NATICK, MASS.				
CHK					
ENG.	SOC DIP ALLOCATION				
APPRD					E. V.
USED ON 8084-861 & 8093-861	SCALE	SIZE C	DWG. NO. LBD 2282	REV. A	
NEXT ASSY	SHEET 3 OF				

Z	S	J	Y	T	I	H	E	D	C	B	A
74H50	PSAT PT1482B		7474	74174	74174	74174	74174	74153	74H74	7404	74H74	8262
1489			7474	7404	7404	74175	74157	74153	74H00	8262	74H04	8095
1488	PSAR PR1472B		74S112	7497	7497	74174	74157	74153	74H10	8262	8095	8095
1489	7408	7404	7408	7497	7497	74H04	SPARE	74153	8256E	8225	74H04	8262
1489	7474	74174	7474	74174	74174	74H04	74H04	74153	82562	8225	74H04	8095
74151	7474	74174	7474		74174	74175	74161	74153		R3 2K	7442	8095
1488	74155	74175	7408	74154	74161	74175	74161	74153	W134	8225	7442	8262
7438	7432	74175	7474	7408	74153	74175	74161	74153	W135	8225	74H04	8095
	7400	7474	7474	7474	7408	74175	74161	74158	7402	R4 2K	74H04	8095
74158		74174	7474	74S112	7410	74H11	74H08	74H20	7432		74H04	8262
74158	74158	7474	74H11		74H30	74S112	74H00	74H52	74H20	74H04	7442	8094
RES 1K	74158	74H08	7400	74150	74174	74155	7410	74H00	74H00	74H04	7442	74H21
74H01	74175	74157	74H00	74151	74148	74155	7410	74H08	74H52	74H04	74H20	74H11
74H01	74175	7400	74H11	W163	9602	RC120	74H11	74H11	74H52	74H00	74H21	74H01
RES 1K	74157	74175	W151	74S112	7474	74H50	74H11	74H00	74H50	74H08	RZ 2K	74H00
74H08	74175	74157	7486	7400	9602	7408	74H00	74H21	74H53	7400	74H10	74H10
	74175	74157	W144	7404	RC117	74H00	7400	74H00	74S112	74H08	74H11	74H55
RES 1K	74157	7414	W158		9602	7474	74161	74H00		74S112	74H74	74H106
74H08	74175	7400	74H00	RC119	7420	7474	7474	74H08	74H04	7474	74H53	74H74
74H08	74175	74H11	7408	9602	74H53	74155	7474	74174	7400	74H08	74H08	74H04
RES 1K	74157	74175	W148	74H53	7474	74153	7474	7408	74157	74157	74H50	74H20
74H01	74175	74157	74H50	7420	7474	7408	74S112	74174	SPARE	SPARE	74H00	RI 15K
74H01	74175	7486	74S112	W147	7408	74S253	R5 2K	9602		74H00	74H10	74H20
7416	74157	7400	9602	7474	74H00	7408	74H21	7474	SPARE	74H08	74S112	74H04
W149	W146	7404	RC118	9602	74174	7474	74S283	75452	SPARE	7474	74H08	74S112

B1

A1

PRIME COMPUTER INC.
NATICK, MASS.
GOULD
DIP ALLOCATION
E.V.
C LBD 2282
1
2/10/76
A208-202

II-37

LTR	DATE	REVISION	DR.	CK.

B2 … A2 (SOLDER SIDE)

NAME		CONN PIN
VCC1		CA-1
VCC1		CA-2
SHIELD(GND)		CA-3
BPCDCPR+		CA-4
BPCDEN+		CA-5
GND		CA-6
BPCDPNO-		CA-7
BPCDPNA-		CA-8
BPCDPNB-		CA-9
BPCDPNC-		CA-10
BPCDPND-		CA-11
BPCDPNE-		CA-12
BPCDPNF-		CA-13
BPCDPNG-		CA-14
BPCDPNH-		CA-15
BPCIEN+		CA-16
BPCIPNO-		CA-17
BPCIPNA-		CA-18
BPCIPNB-		CA-19
BPCIPNC-		CA-20
BPCIPND-		CA-21
SHIELD(GND)		CA-22
BPCICPN+		CA-23
GND		CA-24
BPCCNI+		CA-25
SHIELD(GND)		CA-26
		CA-27
		CA-28
		CA-29
BPCEOR+		CA-30
		CA-31
		CA-32
		CA-33
		CA-34
		CA-35
		CA-36
		CA-37
BPCIOVI-		CA-38
		CA-39
		CA-40
		CA-41
GND		CA-42
BMCWDLR+		CA-43
		CA-44
		CA-45
		CA-46
BMCWDLL+		CA-47
SHIELD(GND)		CA-48
VCC1		CA-49
VCC1		CA-50

NAME		CONN PIN
BMCABL+		CA-51
		CA-52
		CA-53
		CA-54
		CA-55
BMAPEL+		CA-56
BMAPER+		CA-57
BMDPEL-		CA-58
BMDPER-		CA-59
GND		CA-60
BMD01+		CA-61
BMD02+		CA-62
BMD03+		CA-63
BMD04+		CA-64
BMD05+		CA-65
BMD06+		CA-66
BMD07+		CA-67
BMD08+		CA-68
BMD09+		CA-69
BMD10+		CA-70
BMD11+		CA-71
BMD12+		CA-72
BMD13+		CA-73
BMD14+		CA-74
BMD15+		CA-75
BMD16+		CA-76
BMDLP-		CA-77
BMDRP-		CA-78
BMCSELO-		CA-79
GND		CA-80
BMCSELB-		CA-81
BMCSELV-		CA-82
BMCDIN+		CA-83
BMCWRB-		CA-84
BMCWLB-		CA-85
BMCRFSH-		CA-86
BMCEXS1-		CA-87
BMCWSTRB-		CA-88
BMCEXS2-		CA-89
BPCFCLK+		CA-90
BMCSS01-		CA-91
BPCIRQ-		CA-92
BMCSS02-		CA-93
BPCDRQ-		CA-94
BMCSS03-		CA-95
BMCPRCH-		CA-96
BMCCNBL-		CA-97
GND		CA-98
VCC2		CA-99
VCC2		CA-100

NAME		CONN PIN
VCC1		CB-1
VCC1		CB-2
GND		CB-3
ISO(SPARE)		CB-4
BMA99-		CB-5
BMA00-		CB-6
BMA01-		CB-7
BMA02-		CB-8
BMA03-		CB-9
BMA04-		CB-10
BMA05-		CB-11
BMA06-		CB-12
BMA07-		CB-13
BMA08-		CB-14
BMA09-		CB-15
BMA10-		CB-16
BMA11-		CB-17
BMA12-		CB-18
BMA13-		CB-19
BMA14-		CB-20
BMA15-		CB-21
BMA16-		CB-22
BMALP-		CB-23
BMARP-		CB-24
HPWRFL-		CB-25
GND		CB-26
VCORE1		CB-27
VCORE1		CB-28
BPAO1+		CB-29
GND		CB-30
BPAO2+		CB-31
BPAO3+		CB-32
BPAO4+		CB-33
BPAO5+		CB-34
BPAO6+		CB-35
BPAO7+		CB-36
BPAO8+		CB-37
BPAO9+		CB-38
BPAI0+		CB-39
BPAI1+		CB-40
HSYSCLR-		CB-41
GND		CB-42
VCORE2		CB-43
VCORE2		CB-44
BPDPEL-		CB-45
GND		CB-46
BPDPER-		CB-47
BPAPEL-		CB-48
BPA99+		CB-49
BPA00+		CB-50

NAME		CONN PIN
BPAI2+		CB-51
BPAI3+		CB-52
BPAI4+		CB-53
BPAI5+		CB-54
BPAI6+		CB-55
BPAIP+		CB-56
GND		CB-57
BPARP+		CB-58
BPCPIO+		CB-59
BPAPER-		CB-60
BPC60CY+		CB-61
BPCREDY-		CB-62
BPDLP+		CB-63
		CB-64
BPD01+		CB-65
BPDRP+		CB-66
BPD02+		CB-67
BPD03+		CB-68
BPD04+		CB-69
BPD05+		CB-70
BPD06+		CB-71
BPD07+		CB-72
BPD08+		CB-73
BPD09+		CB-74
BPD10+		CB-75
BPD11+		CB-76
VI2-		CB-77
VI2-		CB-78
BPD12+		CB-79
GND		CB-80
BPD13+		CB-81
BPD14+		CB-82
BPD15+		CB-83
BPD16+		CB-84
BPCMOD0+		CB-85
BPCMOD1+		CB-86
BPCMOD2+		CB-87
BPCMOD3+		CB-88
BPCINMD+		CB-89
BPCSCLK+		CB-90
VI2+		CB-91
VI2+		CB-92
HRUN-		CB-93
HRUN-		CB-94
BPCSTRB+		CB-95
GND		CB-96
VSS		CB-97
VSS		CB-98
VBB		CB-99
VBB		CB-100

F2 … C2 (SOLDER SIDE)

NAME		CONN PIN
EIAC4+		CC-1
GND		CC-2
EIAC3+		CC-3
GND		CC-4
EIAC3+		CC-5
GND		CC-6
EIAC2+		CC-7
GND		CC-8
EIAC1+		CC-9
GND		CC-10
TXEIAB-		CC-11
GND		CC-12
TXEIA4-		CC-13
GND		CC-14
TXEIA1-		CC-15
GND		CC-16
TXEIA2-		CC-17
GND		CC-18
EIAC1+		CC-19
GND		CC-20
INBIT3-		CC-21
GND		CC-22
INBIT4-		CC-23
GND		CC-24
INBIT3-		CC-25
GND		CC-26
INBIT2-		CC-27
GND		CC-28
INBIT1-		CC-29
GND		CC-30
INBIT1-		CC-31
GND		CC-32
RXEIA1+		CC-33
GND		CC-34
RXEIA2+		CC-35
GND		CC-36
PREXCL+		CC-37
GND		CC-38
RXEIA3+		CC-39
GND		CC-40
RXEIA4+		CC-41
GND		CC-42
PTEXCL+		CC-43
GND		CC-44

NAME		CONN PIN
RXEIA1+		CD-1
GND		CD-2
CLIN+		CD-3
		CD-4
CLIN+		CD-5
		CD-6
CLIN+		CD-7
		CD-8
TXCL2-		CD-9
		CD-10
TXCL1-		CD-11
		CD-12
TXCL3-		CD-13
GND		CD-14
TXCL4-		CD-15
		CD-16
		CD-17
		CD-18
TXCLR2+		CD-19
		CD-20
TXCLR1+		CD-21
		CD-22
TXCLR3+		CD-23
		CD-24
TXCLR4+		CD-25
		CD-26
		CD-27
		CD-28
		CD-29
		CD-30
EXTCLK+		CD-31
		CD-32
SCOPECY		CD-33
		CD-34
WDTTST		CD-35
		CD-36
WDTEXS-		CD-37
		CD-38
RETOUT-		CD-39
		CD-40
EXPFI-		CD-41
		CD-42
RETIN-		CD-43
		CD-44

NAME		CONN PIN
B20D01+		CE-1
GND		CE-2
B20D02+		CE-3
GND		CE-4
B20D03+		CE-5
GND		CE-6
B20D04+		CE-7
GND		CE-8
B20D05+		CE-9
GND		CE-10
B20D06+		CE-11
GND		CE-12
B20D07+		CE-13
GND		CE-14
B20D08+		CE-15
GND		CE-16
B20D09+		CE-17
GND		CE-18
B20D10+		CE-19
GND		CE-20
B20D11+		CE-21
GND		CE-22
B20D12+		CE-23
GND		CE-24
B20D13+		CE-25
GND		CE-26
B20D14+		CE-27
GND		CE-28
B20D15+		CE-29
GND		CE-30
B20D16+		CE-31
GND		CE-32
DESKS		CE-33
GND		CE-34
D2MVF		CE-35
GND		CE-36
D2RDY		CE-37
GND		CE-38
D2OTA		CE-39
GND		CE-40
D2STRB		CE-41
GND		CE-42
D2MVR		CE-43
GND		CE-44

NAME		CONN PIN
D10D01+		CF-1
GND		CF-2
B10D02+		CF-3
GND		CF-4
B10D03+		CF-5
GND		CF-6
B10D04+		CF-7
GND		CF-8
B10D05+		CF-9
GND		CF-10
B10D06+		CF-11
GND		CF-12
B10D07+		CF-13
GND		CF-14
B10D08+		CF-15
GND		CF-16
B10D09+		CF-17
GND		CF-18
B10D10+		CF-19
GND		CF-20
B10D11+		CF-21
GND		CF-22
B10D12+		CF-23
GND		CF-24
B10D13+		CF-25
GND		CF-26
B10D14+		CF-27
GND		CF-28
B10D15+		CF-29
GND		CF-30
B10D16+		CF-31
GND		CF-32
DISKS		CF-33
GND		CF-34
DIMVF		CF-35
GND		CF-36
DIRDY		CF-37
GND		CF-38
DIOTA		CF-39
GND		CF-40
DISTRB		CF-41
GND		CF-42
DIMVR		CF-43
GND		CF-44

IV-38

MATERIAL	DWN Ledar 2/9/76	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	CONNECTOR SIGNAL(E.V.) NAME LIST, SOC
	APPRD	
	USED ON NEXT ASSY	SCALE — SIZE C DWG. NO. LBD2232 REV. 1 SHEET 34 OF 34

PRIME COMPUTER, INC.
FRAMINGHAM, MASS

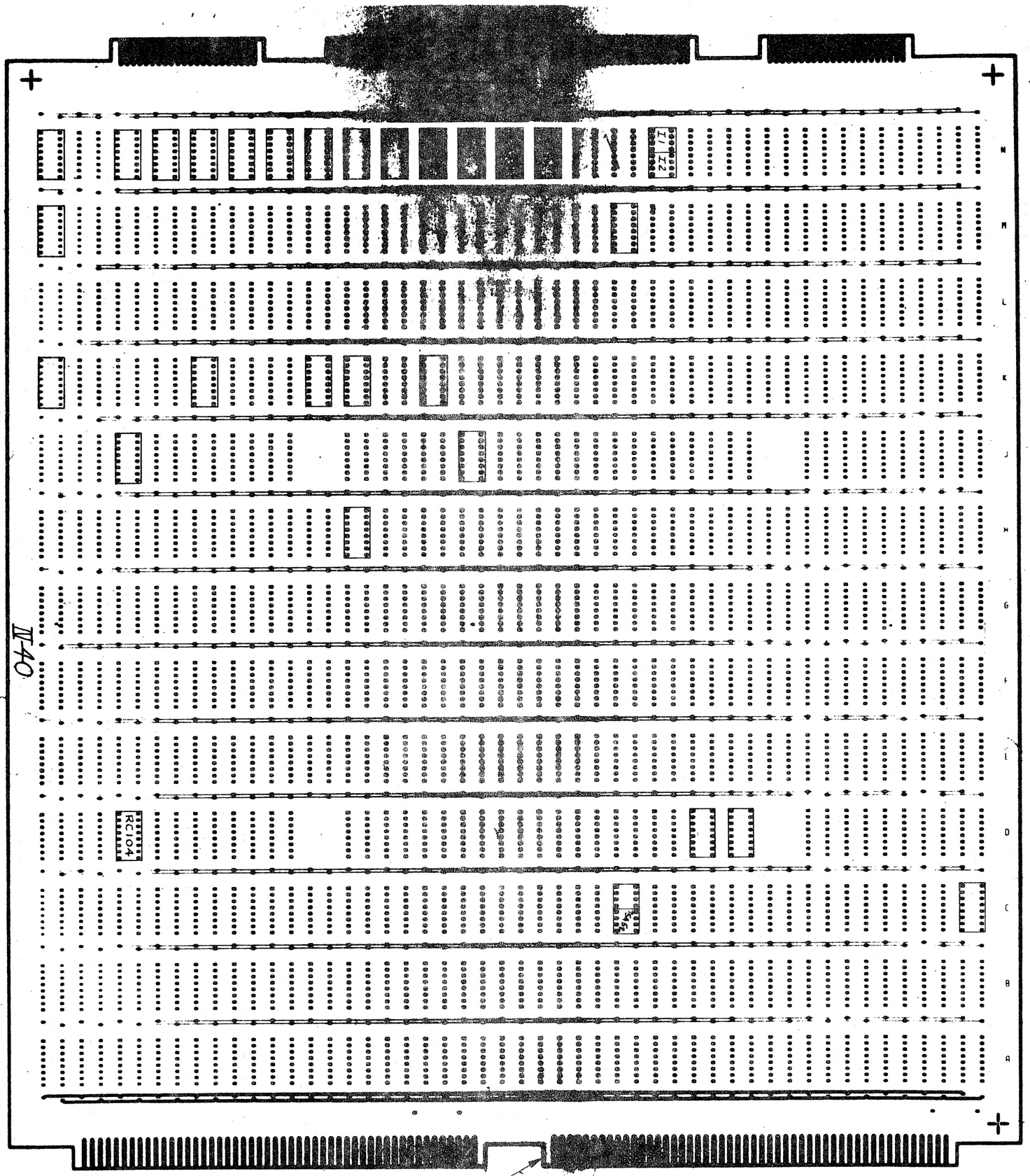
SOC ASSEMBLY E.V.
SLC OPTION

SIZE NONE
SHEET 41

DWG NO
C LBD2282

REV
1

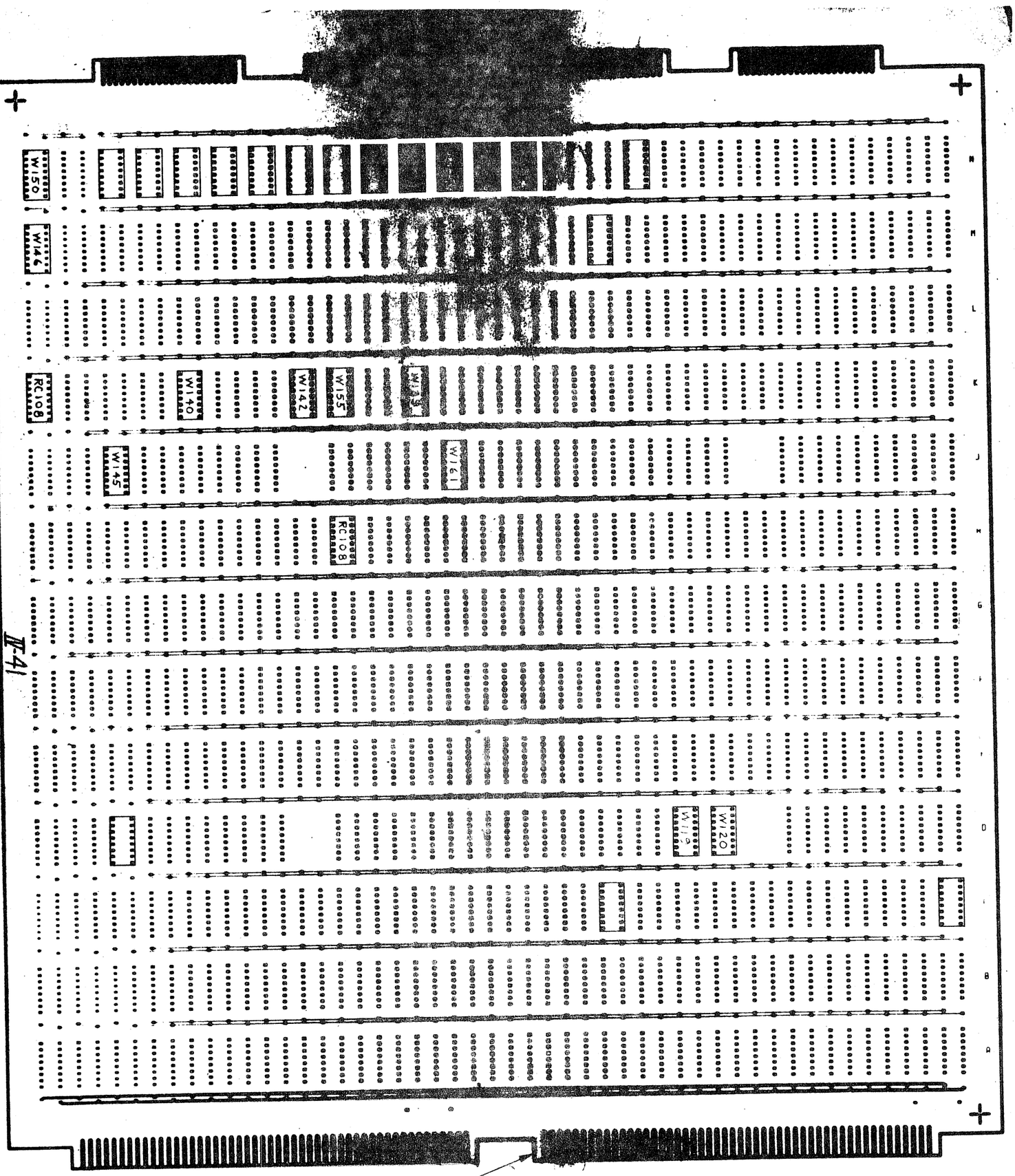
PREREQUISITE
3006-901
3007-901
3008-902
3009-902
ANY



PREREQUISITE

ANY
- 3006-901
- 3007-901
- 3008-902
- 3009-902

MATERIAL	DRAWN Mahler 2/10/76	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED: - REMOVE ALL BURRS AND SHARP EDGES - INTERPRET DIMS AND TOLERANCES PER ANSI Y14.5	CHK	SOC ASSEMBLY E.V WDT OPTION
	ENGR	
	APPVD	
	USED ON NEXT ASSY	SIZE C / DWG NO LBD2282 / REV 1
		SCALE 1/2 / SHEET

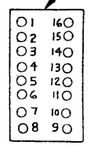


II-41

PREREQUISITE
3007-901

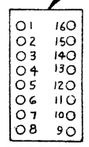
	DWN Lador 2/10/76	PRIME COMPUTER, INC. FRAMINGHAM, MASS
	CHK	
	ENG	SOC ASSEMBLY E.V
	APPROV	RTC/ALC/16 BIT BP/DMA/PIC
		BPIOC OPTION
	SIZE	SCALE NONE
	SHEET 43 OF	C 1BD2282 1

CON1719-001 (REF)



HEADER DIP A (SITE 35D)

CON1719-001 (REF)



HEADER DIP B (SITE 37D)

HEADER DIP A OPTIONS 3006, 3007 (ALC(TTY) & SLC)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
12		1	00 - 07
12		2	10 - 17
12		3	20 - 27
12		4	30 - 37
12		5	40 - 47
12		6	50 - 57
12		7	60 - 67
12	TO	9	70 - 77

HEADER DIP A OPTIONS 3006 (PTR) 3007 (BPIOC)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
13		1	00-07
13		2	10-17
13		3	20-27
13		4	30-37
13		5	40-47
13		6	50-57
13		7	60-67
13	TO	9	70-77

HEADER DIP A OPTIONS 3006 (PTP) 3025 (2ND BPIOC)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
14		1	00-07
14		2	10-17
14		3	20-27
14		4	30-37
14		5	40-47
14		6	50-57
14		7	60-67
14	TO	9	70-77

HEADER DIP A OPTIONS 3006, 3007 (RTC, PRTC (PIC), WDT)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
15		1	00-07
15		2	10-17
15		3	20-27
15		4	30-37
15		5	40-47
15		6	50-57
15		7	60-67
15	TO	9	70-77

HEADER DIP B OPTIONS 3006, 3007 (ALC (TTY) & SLC)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
12		1	0,10,20,30,40,50,60,70
12		2	1,11,21,31,41,51,61,71
12		3	2,12,22,32,42,52,62,72
12		4	3,13,23,33,43,53,63,73
12		5	4,14,24,34,44,54,64,74
12		6	5,15,25,35,45,55,65,75
12		7	6,16,26,36,46,56,66,76
12	TO	9	7,17,27,37,47,57,67,77

FOR DEFAULT:
DEVICE ADDRESS = 04
35D-12 TO 35D-01
37D-12 TO 37D-05

3008 - 3009
FOR MANUFACTURING TEST
ADDRESS = 71
35D-12 TO 35D-09
37D-12 TO 37D-02

HEADER DIP B OPTIONS 3006 (PTR) 3007 (BPIOC)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
13		1	0,10,20,30,40,50,60,70
13		2	1,11,21,31,41,51,61,71
13		3	2,12,22,32,42,52,62,72
13		4	3,13,23,33,43,53,63,73
13		5	4,14,24,34,44,54,64,74
13		6	5,15,25,35,45,55,65,75
13		7	6,16,26,36,46,56,66,76
13	TO	9	7,17,27,37,47,57,67,77

3006 (PTR)
FOR DEFAULT:
DEVICE ADDRESS = 01
35D-13 TO 35D-01
37D-13 TO 37D-02

3007 (BPIOC)
FOR DEFAULT:
DEVICE ADDRESS = 30
35D-13 TO 35D-02
37D-13 TO 37D-01

3008 & 3009
FOR DEFAULT
ADDRESS = 33
35D-13 TO 35D-04
37D-13 TO 37D-04

HEADER DIP B OPTIONS 3006 (PTP) 3025 (2ND BPIOC)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
14		1	0,10,20,30,40,50,60,70
14		2	1,11,21,31,41,51,61,71
14		3	2,12,22,32,42,52,62,72
14		4	3,13,23,33,43,53,63,73
14		5	4,14,24,34,44,54,64,74
14		6	5,15,25,35,45,55,65,75
14		7	6,16,26,36,46,56,66,76
14	TO	9	7,17,27,37,47,57,67,77

3006 (PTP)
FOR DEFAULT:
DEVICE ADDRESS = 02
35D-14 TO 35D-01
37D-14 TO 37D-03

3025 (2ND BPIOC)
FOR DEFAULT:
DEVICE ADDRESS = 31
35D-14 TO 35D-04
37D-14 TO 37D-02

3008 & 3009
FOR DEFAULT
ADDRESS = 34
35D-14 TO 35D-04
37D-14 TO 37D-05

HEADER DIP B OPTIONS 3006, 3007 (RTC, PRTC (PIC), WDT)			
JUMPER			DEVICE ADDRESS
PIN	TO	PIN	
15		1	0,10,20,30,40,50,60,70
15		2	1,11,21,31,41,51,61,71
15		3	2,12,22,32,42,52,62,72
15		4	3,13,23,33,43,53,63,73
15		5	4,14,24,34,44,54,64,74
15		6	5,15,25,35,45,55,65,75
15		7	6,16,26,36,46,56,66,76
15	TO	9	7,17,27,37,47,57,67,77

FOR DEFAULT:
DEVICE ADDRESS = 20
35D-15 TO 35D-03
37D-15 TO 37D-01

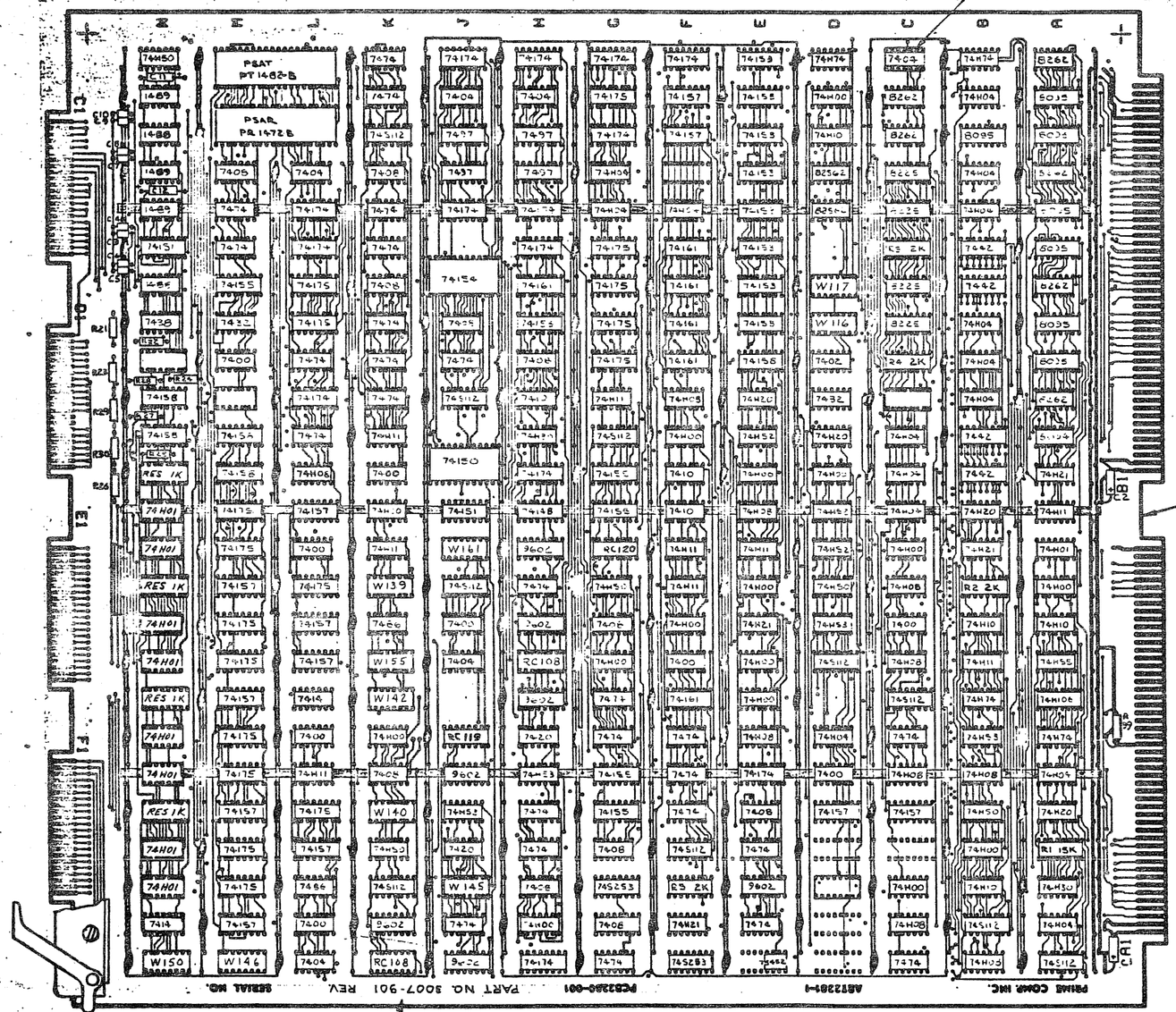
3008 & 3009
FOR MANUFACTURING TEST
ADDRESS = 70
35D-15 TO 35D-09
37D-15 TO 37D-01

MATERIAL	DWN Linder 2/9/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	SOC DEVICE ADDRESS CONFIGURATION E.V.	
	APPRD		
	USED ON	SCALE	SIZE C
	NEXT ASSY	SHEET 47 OF	DWG. NO. LBD2282 REV. 2

PDF-003

NO	LTR	DATE	REVISION	BY	CHK
	A	8/1/74	RELEASED		
	B	3/11/74	PER ECR 1729		

REMOVE THIS DIP FROM 1 BOARD WHEN 2 OR MORE SOC BOARDS ARE IN THE SAME SYSTEM



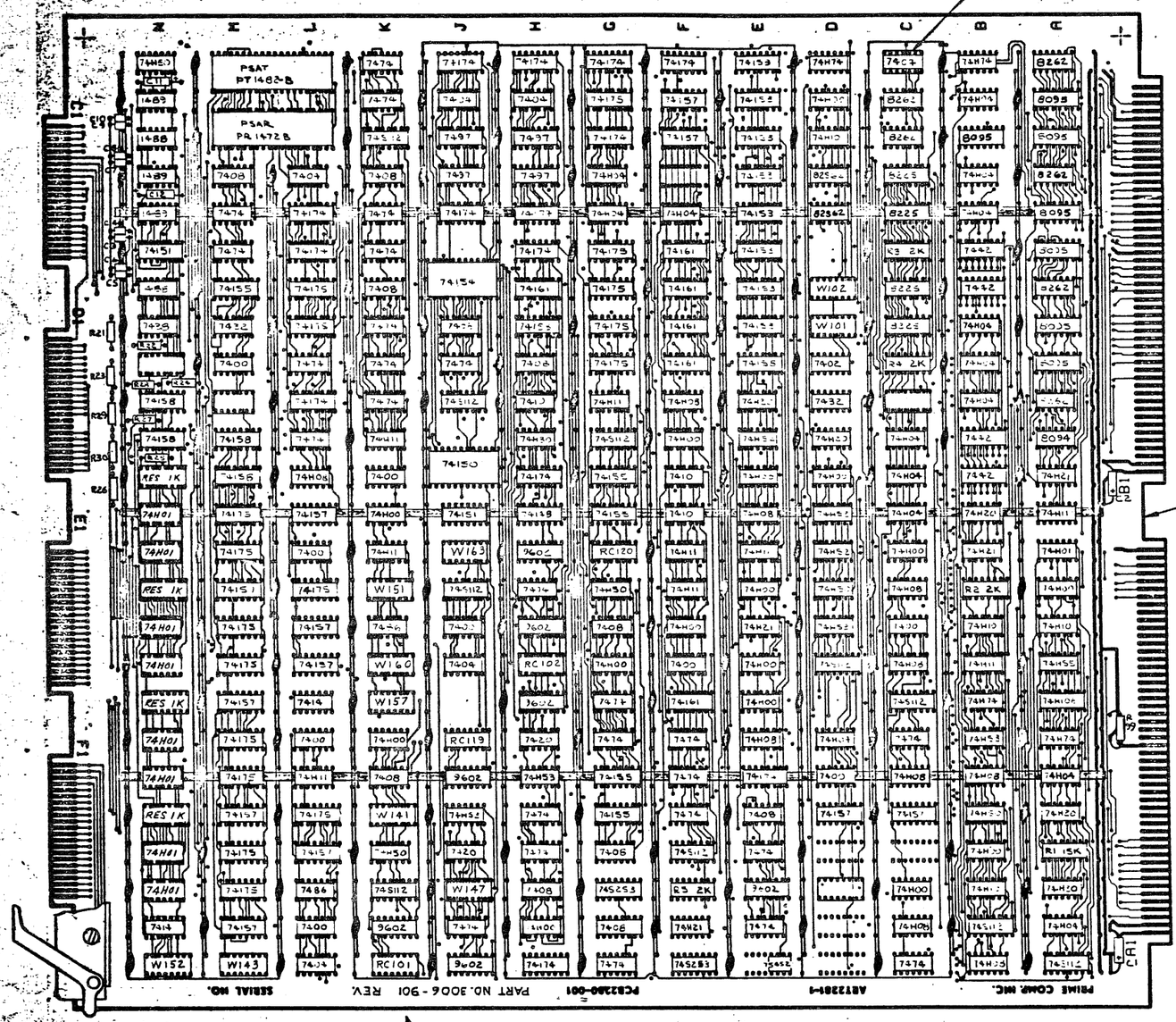
3007-901 COMPONENTS	LOCATION
RC 108	1K
RC 109	17M
W 116	35D
W 117	37D
W 189	21K
W 140	9K
W 142	15K
W 145	5J
W 146	1M
W 150	1N
W 155	17K
W 161	23J
74H01	4R, 7N, 11M, 18N 17N, 19N, 25 N&P
RES 1K	9N, 15N, 21N, 27N

STAMP PART NO. & REV. IN BLACK AS SHOWN

MATERIAL SEE BOM	DWN 10/20/75	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ±.03 .XXX ±.005 ANGLES ±1/2°	CHK 12/24/75	SOC ASSEMBLY E.V RTC/ALC/16 BIT BP/DMA/PIC (BPIOC)	
	ENG 12-24-75		
	APPRO		
	USED ON NEXT ASSY	SCALE NONE SHEET 1 OF 1	SIZE D DWG NO 3007-901 REV B

M	LTR	DATE	REVISION	DR.	CK.
	A	12/5/75	RELEASED	JCL	JCL
	B	2/17/76	PER ECR 1729	JTS	CCV

REMOVE THIS DIP FROM 1 BOARD WHEN 2 OR MORE SOC BOARDS ARE IN THE SAME SYSTEM.



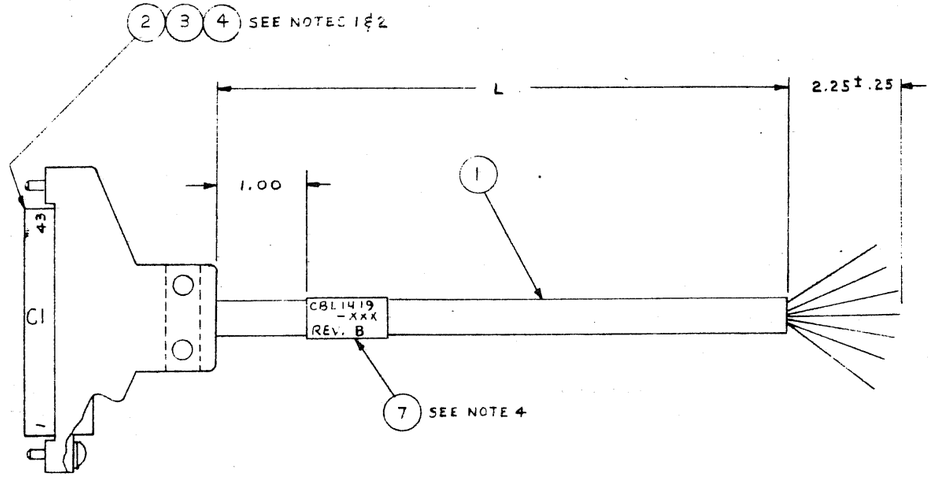
3006-901 COMPONENTS	LOCATION
RC101	1K
RC102	17H
W101	35D
W102	37D
W141	9K
W143	1M
W147	5J
W151	21K
W152	1N
W157	15K
W160	17K
W163	23J
74H01	5N, 7N, 11N, 13N, 17N, 19N, 23N, 25N
RES 1K	9N, 15N, 21K, 27N

STAMP PART NO. & REV. IN BLACK AS SHOWN

MATERIAL SEE BOM	DWN 10/17/75	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK 12/31/75	SOC ASSEMBLY E.V. RTC/AL/PTR-P/DMA/FIC	
	ENG. 12-29-75	SCALE NONE	SIZE D DWG. NO. 3006-901 REV. B
	APPRO	SHEET 1 OF 1	
	USED ON NEXT ASSY		

WIRE LIST				COMMENTS
FROM	TO	BASE COLOR	STRIPE COLOR	
C1-01	OPEN END	BLK	—	TP
C1-02		WHT	—	
C1-03		YEL	—	
C1-04		ORG	—	
C1-05		GRN	—	
C1-06		GRY	—	
C1-07		BLK	WHT	
C1-08		BLK	RED	
C1-09		BLK	GRN	
C1-10		BLK	ORG	
C1-11		BLK	YEL	
C1-12		BLK	BLUE	
C1-13		WHT	BLK	
C1-14		WHT	RED	
C1-15		WHT	GRN	
C1-16		WHT	ORG	
C1-17		WHT	BLUE	
C1-18		WHT	YEL	
C1-19		WHT	BRWN	
C1-20		WHT	GRY	
C1-21		YEL	BLK	
C1-22		YEL	RED	
C1-23		YEL	GRN	
C1-24		YEL	BLUE	
C1-25		YEL	BRWN	
C1-26		YEL	GRY	
C1-27		ORG	BLK	
C1-28		ORG	RED	
C1-29		ORG	GRN	
C1-30		ORG	BLUE	
C1-31		ORG	BRWN	
C1-32		ORG	GRY	
C1-33		GRN	BLK	
C1-34		GRN	RED	
C1-35		GRN	WHT	
C1-36		GRN	BLUE	
C1-37		GRN	BRWN	
C1-38		GRN	YEL	
C1-39		GRN	GRY	
C1-40		GRY	BLK	
C1-41		GRY	RED	
C1-42		GRY	WHT	
C1-43		GRY	YEL	TP
C1-44	OPEN END	GRY	ORG	

LTR	DATE	REVISION	DR.	CK.
A	12/10/73	RELEASED	—	—
B	6/3/75	PER ECN 1606	MB	JCL



DASH NO.	L DIM
-001	25' 0"
-002	10' 0"

NOTES:-
1. STAMP MARKING C1 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM 4 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 2.
3. INSTALL ITEM 10 IN CUTOUT OF ITEM 6 TO INSURE TIGHT FIT OF CABLE.
4. TYPE PART NO. & REVISION IN BLACK ON ITEM 7.

MATERIAL: SEE BOM	DWN: St. Bergan 12/7/73	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ± .02, XXX ± .005, ANGLES ± 1/2°	CHK: J.C. Lee 6/24/75	CABLE, CBLGP
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE NONE SHEET 1 OF 1 — SIZE C — DWG. NO. CBL1419-XXX — REV. B

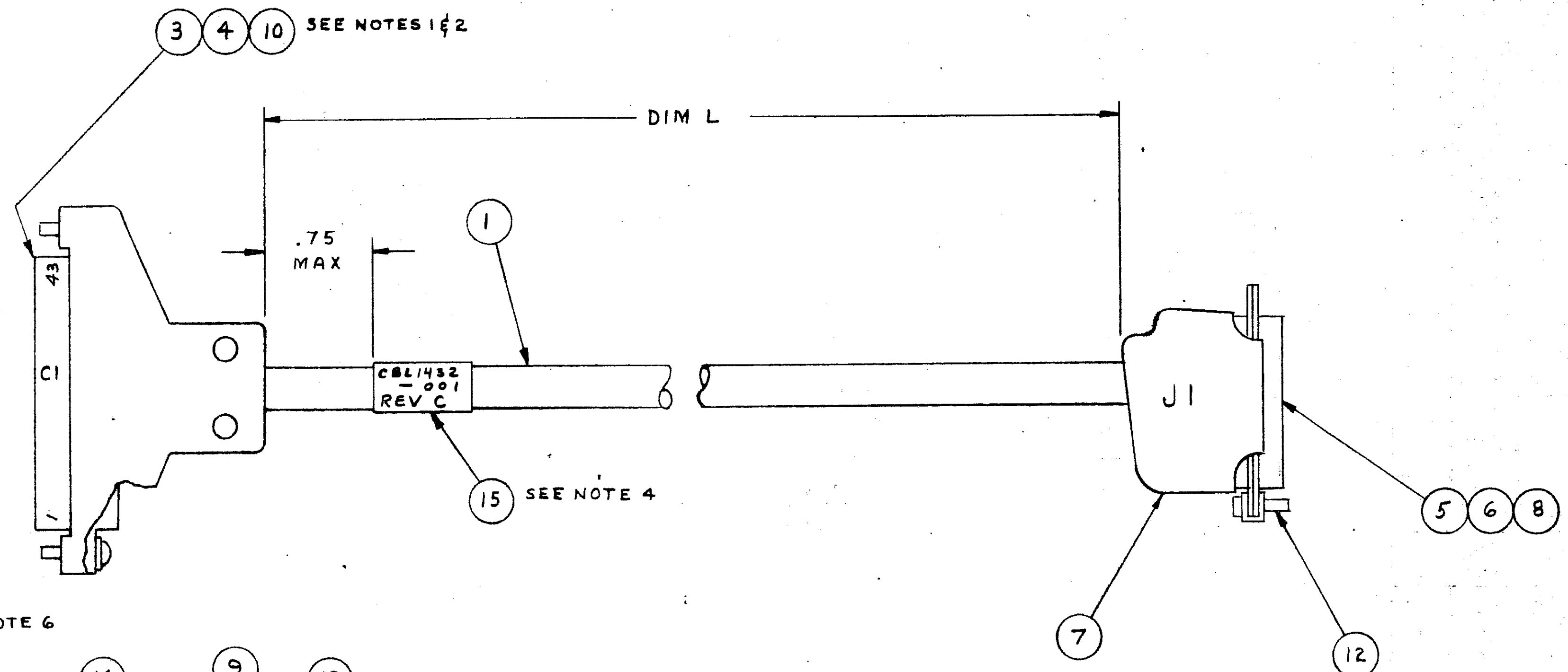
CBL1419-XXX

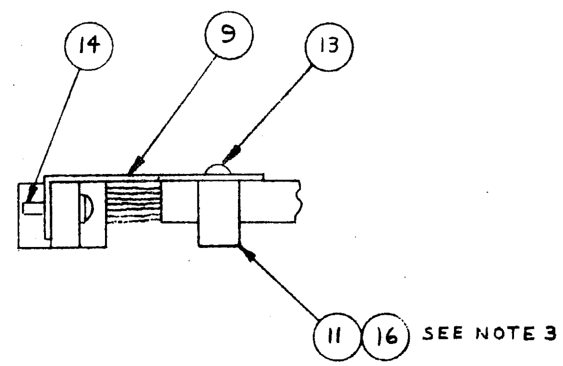
LTR	DATE	REVISION	DR.	CK.
A	[illegible]/74	RELEASED	—	—
B	3/17/75	ECN 1555	[illegible]	M.S.
C	6/3/75	PER ECN 1606	[illegible]	[illegible]

WIRE LIST

FROM:	TO	BASE COLOR	STRIPE COLOR	COM-MENTS
C1-01	J1-08	BLK	—	TP
C1-02	J1-25*	WHT	—	
C1-03	J1-07	YEL	—	
C1-04	J1-25*	ORG	—	
C1-05	J1-06	GRN	—	
C1-06	J1-25*	GRY	—	
C1-07	J1-05	BLK	WHT	
C1-08	J1-25*	BLK	RED	
C1-09	J1-04	BLK	GRN	
C1-10	J1-25*	BLK	ORG	
C1-11	J1-03	BLK	YEL	
C1-12	J1-25*	BLK	BLUE	
C1-13	J1-02	WHT	BLK	
C1-14	J1-25*	WHT	RED	
C1-15	J1-01	WHT	GRN	
C1-16	J1-25*	WHT	ORG	
		WHT	BLUE	
		WHT	YEL	
		WHT	BRWN	
		WHT	GRY	
		YEL	BLK	
		YEL	RED	
		YEL	GRN	
		YEL	BLUE	
		YEL	BRWN	
		YEL	GRY	
		ORG	BLK	
		ORG	RED	
		ORG	GRN	
		ORG	BLUE	
		ORG	BRWN	
		ORG	GRY	
C1-33	J1-13	GRN	BLK	
C1-34	J1-25*	GRN	RED	
C1-35	J1-11	GRN	WHT	
C1-36	J1-25*	GRN	BLUE	
		GRN	BRWN	
		GRN	YEL	
		GRN	GRY	
		GRY	BLK	
C1-41	J1-12	GRY	RED	
C1-42	J1-25*	GRY	WHT	
		GRY	YEL	TP
		GRY	ORG	

SEE NOTE 6





NOTES:-
1. STAMP MARKINGS C1, J1 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM 10 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 3
3. INSTALL ITEM 11 IN CUTOUT OF ITEM 16 TO INSURE TIGHT FIT OF CABLE.
4. TYPE PART NO. & REVISION IN BLACK ON ITEM 15
5. ALL UNUSED WIRES ARE TO BE CUT OFF AND TERMINATED INSIDE CABLE.
6. ALL WIRES MARKED * TO BE PIG TAILED WITH ITEM 2 AND CONNECTED TO J1-25.
7. SEE DWG C INS1210 FOR CABLE CODING LOCATION.
8. FOR SIGNAL NAMES SEE LBD1528

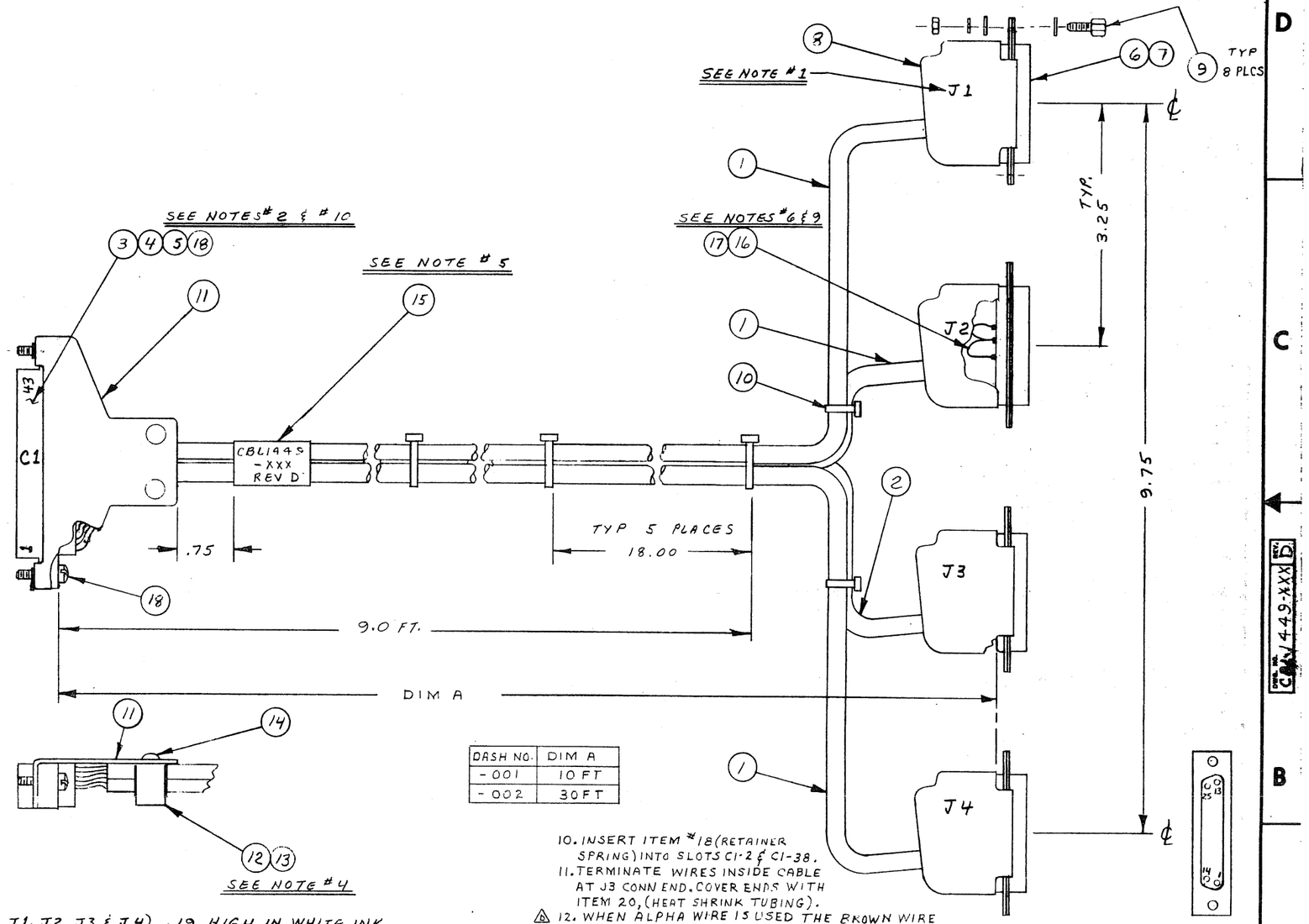
-XXX	DIM L	TOL
-001	10 FT	± 6 IN.

MATERIAL: SEE BOM	DWN: [illegible] 5/9/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES	CHK: [illegible] 7/12/74	CABLE PTP TO TOC
	ENG: [illegible] 7-15-74	
	APPD: [illegible]	
		SCALE NONE — SHEET 1 OF 1 — SIZE C — CBL 1432-XXX — REV C

I-02

WIRE LIST			COMMENTS	JUMPER	DEVICE
FROM	TO	COLOR			
C1-15	J1-3	GRN	5 WIRE CABLE		
C1-16	J1-7	BLK			
C1-33	J1-2	RED			
C1-9	J1-9	BRN			
C1-29	J1-5	WHITE			
C1-17	J2-3	GRN	5 WIRE CABLE	J2-6 TO J2-8** TO J2-20 SEE NOTES #6 & #9	CENTRONICS LINE PRINTER
C1-18	J2-7	BLK			
C1-35	J2-2	RED			
C1-7	J2-9	BRN			
C1-27	J2-11	WHITE			
C1-11	J3-3	GRN	10 WIRE CABLE	J3-4 TO J3-5 & J3-8* TO J3-20 SEE NOTES 6 & 7	INFOTON CRT DISPLAY
C1-39	J3-2	RED			
C1-5	J3-9	BRN			
C1-25	J3-8*	WHITE			
C1-19	J3-12	ORN			
C1-31	J3-11	YEL			
C1-37	**	BLU			
C1-38	J3-7*	GRAY			
C1-43	**	PURPLE			
C1-44	J3-7*	BLK			
C1-13	J4-3	GRN	5 WIRE CABLE	J4-4 TO J4-5 & J4-6* TO J4-20 SEE NOTE #6,7	DOCUMENTATION CARD READER
C1-14	J4-7	BLK			
C1-41	J4-2	RED			
C1-1	J4-9	BRN			
C1-23	J4-6*	WHITE			

LTR	DATE	REVISION	DR.	CK.
A	5/29/73	REVISED PER ECN 1303		
B	4/13/74	REDESIGNED PER ECN 1312 & 1375	JPL	
C	7/19/74	REVISED PER ECN 1422 & 1450	WG	JPL
D	9/15/75	PER ECN 1628	WG	JPL



DASH NO.	DIM A
-001	10 FT
-002	30 FT

NOTES:

1. STAMP MARKINGS (C1, J1, J2, J3 & J4) .19 HIGH IN WHITE INK. POSITION APPROXIMATELY AS SHOWN.
2. INSERT KEY (ITEM # 5) BETWEEN SLOTS 25/26 & 27/28 OF ITEM # 3.
3. EQUIVALENT CONNECTORS MAY BE SUBSTITUTED.
4. WRAP ITEM # 13 (TAPE) AROUND ITEMS #1 & # 2 TO PROVIDE CLAMPING ACTION WITH ITEMS #11 & # 12 AS SHOWN.
5. TYPE PART NO & REV. IN BLACK ON ITEM # 15 AS SHOWN
6. INSERT ITEMS # 17 (*28-24) SOCKETS IN J2-6, J2-20, J3-4, J3-5, J3-20, J4-4, J4-5 & J4-20.
7. * PIG TAIL LEADS INDICATED * WITH ITEM # 16. USE ITEM #17 (SOCKETS) AT J3-7 & J4-6
8. FOR SIGNAL NAMES REFER TO LBD0549.
9. ** DOUBLE CRIMP WIRES IN J2-8 AS INDICATED BY **. [CRIMP NEST 24-20 (RED) IS RECOMMENDED FOR DOUBLE WIRE CRIMPS]
10. INSERT ITEM #18 (RETAINER SPRING) INTO SLOTS C1-2 & C1-38.
11. TERMINATE WIRES INSIDE CABLE AT J3 CONN END. COVER ENDS WITH ITEM 20, (HEAT SHRINK TUBING).
12. WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

I-03

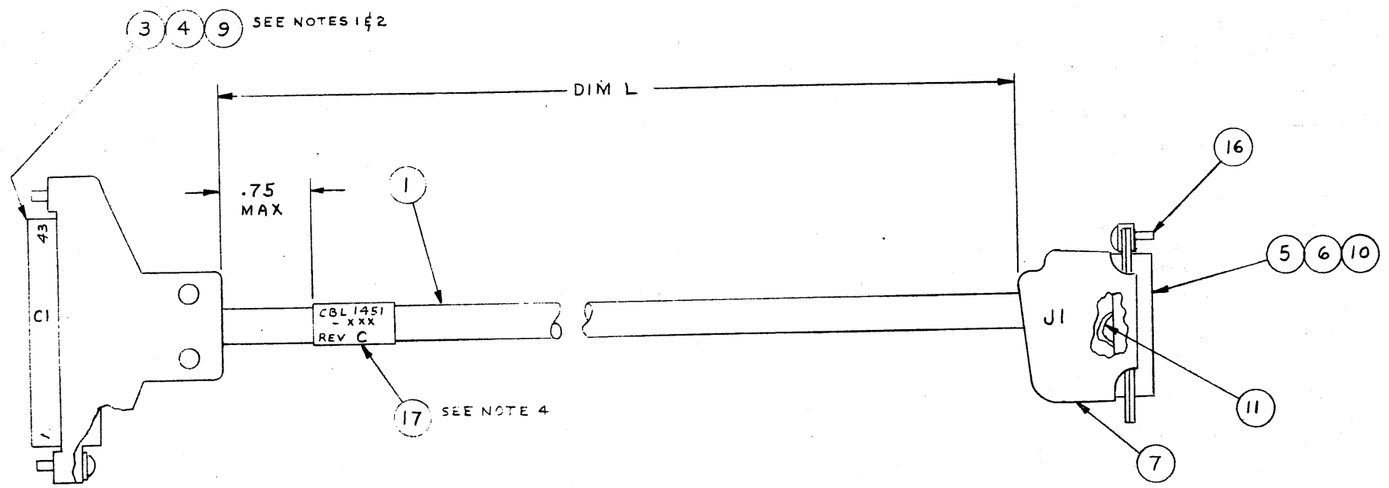
MATERIAL SEE BOM WAS 28L00-001	DWN J.G.L. 12/29/72	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK. [illegible]	CABLE, OPT A/SOC WITH 4 EIA CONN.
	ENG. [illegible]	
	APPRD	
	USED ON NEXT ASSY 3129	SCALE NONE SHEET 1 OF 1 SIZE C DWG. NO. CBL1449-XXX REV. D

DWG. NO. CBL1449-XXX REV. D

LTR	DATE	REVISION	DR.	CK.
A	7/8/74	RELEASED	—	—
B	3/17/75	ECN 1555	JAB	M.G.
C	4/3/75	PER ECN 1606	JAB	JPL

WIRE LIST

FROM	TO	BASE COLOR	STRIPE COLOR	COMMENTS
C1-01	J1-08	BLK	—	TP
C1-02	J1-11 **	WHT	—	
C1-03	J1-07	YEL	—	
C1-04	J1-11 **	ORG	—	
C1-05	J1-06	GRN	—	
C1-06	J1-11 **	GRY	—	
C1-07	J1-05	BLK	WHT	
C1-08	J1-11 **	BLK	RED	
C1-09	J1-04	BLK	GRN	
C1-10	J1-11 **	BLK	ORG	
C1-11	J1-03	BLK	YEL	
C1-12	J1-11 **	BLK	BLUE	
C1-13	J1-02	WHT	BLK	
C1-14	J1-11 **	WHT	RED	
C1-15	J1-01	WHT	GRN	
C1-16	J1-11 **	WHT	ORG	
		WHT	BLUE	
		WHT	YEL	
		WHT	BRWN	
		WHT	GRY	
		YEL	BLK	
		YEL	RED	
		YEL	GRN	
		YEL	BLUE	
		YEL	BRWN	
		YEL	GRY	
		ORG	BLK	
		ORG	RED	
		ORG	GRN	
		ORG	BLUE	
		ORG	BRWN	
		ORG	GRY	
C1-33	J1-14	GRN	BLK	
C1-34	J1-11 **	GRN	RED	
C1-35	J1-16	GRN	WHT	
C1-36	J1-11 **	GRN	BLUE	
C1-37	J1-14	GRN	BRWN	
C1-38	J1-11 **	GRN	YEL	
		GRN	GRY	
		GRY	BLK	
C1-41	J1-09	GRY	RED	
C1-42	J1-11 **	GRY	WHT	
C1-43	J1-17	GRY	YEL	TP
C1-44	J1-11 **	GRY	ORG	SEE NOTE 6
J1-10	J1-12	RED		JMPR



NOTES:-
1. STAMP MARKINGS C1, J1 .15 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM 9 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 3.
3. INSTALL ITEM 13 IN CUTOUT OF ITEM 12 TO INSURE TIGHT FIT OF CABLE.
4. TYPE PART NO. & REVISION IN BLACK ON ITEM 17
5. ALL UNUSED WIRES ARE TO BE CUT OFF AND TERMINATED INSIDE CABLE.
6. ALL WIRES MARKED ** TO BE PIG TAILED WITH ITEM 2 AND CONNECTED TO J1-11.
7. SEE DWG C1NS1210 FOR CABLE CODING LOCATION.
8. FOR SIGNAL NAMES SEE LBD 1528

-XXX	DIM L	TOL
-001	10FT	± 6 IN

V-04

MATERIAL: SEE BOM

DWN: JB Bogan 5/8/74
CHK: JC Thurlow 7/14/74
ENG: MM Spar 7-15-74
APPD:
USED ON
NEXT ASSY

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES.
—DIMENSIONS ARE IN INCHES
—TOLERANCES
XX ± .02 XXX ± .005 ANGLES ± 1/2°

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE
PTR TO SOC (R-6375)

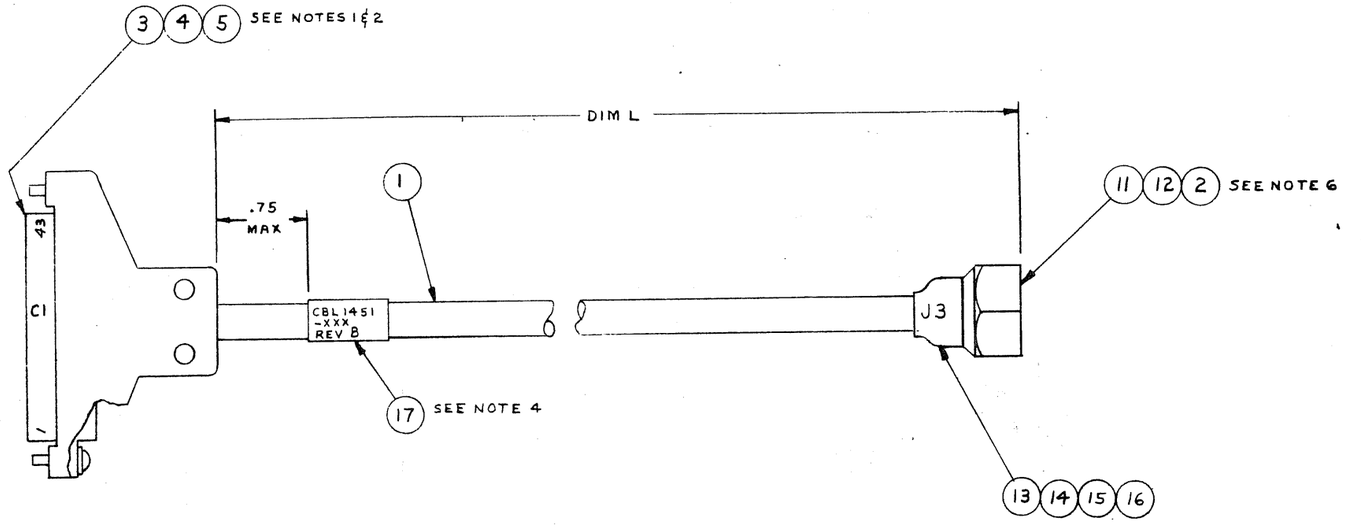
SCALE NONE SHEET 1 OF 1 SIZE C DWG. NO. CBL1451-001 C

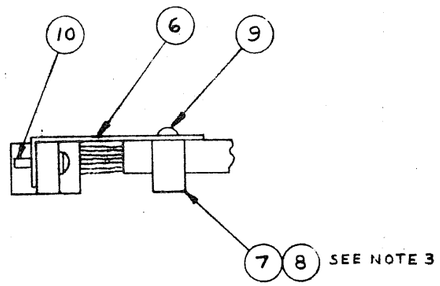
CBL1451-001 C

LTR	DATE	REVISION	DR.	CK.
A	7/8/74	RELEASED	—	—
B	4/3/75	PER ECO 1606	WB	JCL

WIRE LIST

FROM	TO	BASE COLOR	STRIPE COLOR	COMMENTS
C1-01	J3-08	BLK	—	TP
C1-02	J3-10**	WHT	—	
C1-03	J3-07	YEL	—	
C1-04	J3-10**	ORG	—	
C1-05	J3-06	GRN	—	
C1-06	J3-10**	GRY	—	
C1-07	J3-05	BLK	WHT	
C1-08	J3-10**	BLK	RED	
C1-09	J3-04	BLK	GRN	
C1-10	J3-10**	BLK	ORG	
C1-11	J3-03	BLK	YEL	
C1-12	J3-10**	BLK	BLUE	
C1-13	J3-02	WHT	BLK	
C1-14	J3-10**	WHT	RED	
C1-15	J3-01	WHT	GRN	
C1-16	J3-10**	WHT	ORG	
		WHT	BLUE	
		WHT	YEL	
		WHT	BRWN	
		WHT	GRY	
		YEL	BLK	
		YEL	RED	
		YEL	GRN	
		YEL	BLUE	
		YEL	BRWN	
		YEL	GRY	
		ORG	BLK	
		ORG	RED	
		ORG	GRN	
		ORG	BLUE	
		ORG	BRWN	
		ORG	GRY	
		GRN	BLK	
		GRN	RED	
C1-35	J3-12	GRN	WHT	
C1-36	J3-10**	GRN	BLUE	
C1-37	J3-15	GRN	BRWN	
C1-38	J3-10**	GRN	YEL	
		GRN	GRY	
		GRY	BLK	
C1-41	J3-09	GRY	RED	
C1-42	J3-10**	GRY	WHT	
C1-43	J3-11	GRY	YEL	TP
C1-44	J3-10**	GRY	ORG	





NOTES:-
1. STAMP MARKINGS C1, J3 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM 5 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 3
3. INSTALL ITEM 8 IN CUTOUT OF ITEM 7 TO INSURE TIGHT FIT OF CABLE.
4. TYPE PART NO. & REVISION IN BLACK ON ITEM 17
5. ALL UNUSED WIRES ARE TO BE CUT OFF AND TERMINATED INSIDE CABLE.
6. ALL WIRES MARKED** TO BE PIG TAILED WITH ITEM 2 AND CONNECTED TO J3-10.
7. SEE DWG C INS1210 FOR CABLE CODING LOCATION.
8. FOR SIGNAL NAMES SEE LBD1528.

-XXX	DIM L	TOL
-101	10 FT	± 6 IN.

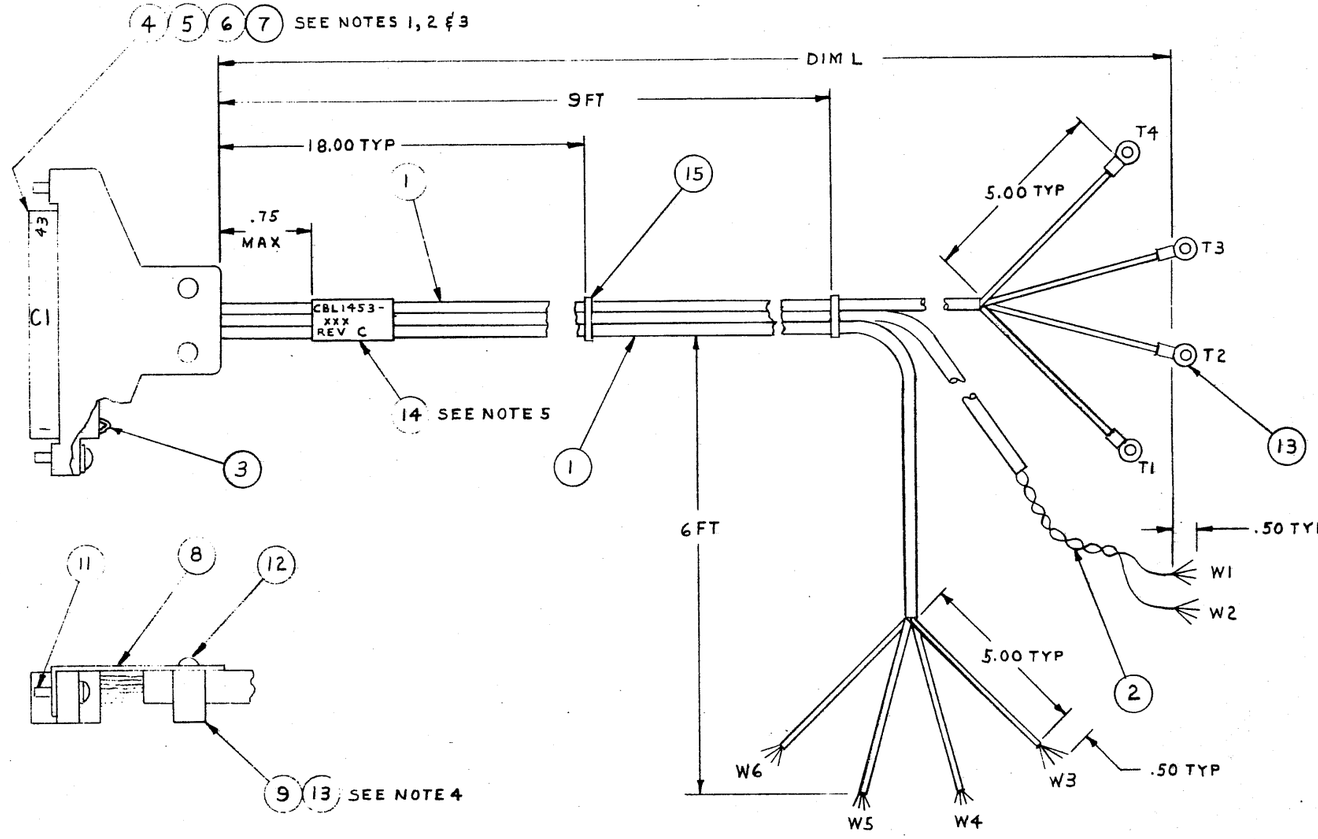
F05

MATERIAL: SEE BOM	DWN: W. Bogan 5/14/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.03 .XXX ±.005 ANGLES ±1/2°	CHK: J. C. MacQuarrie 7/12/74	CABLE, PTR TO SOC (COMBO)
	ENG: M. Soper 7-15-74	
	APPD: [illegible]	
	USED ON / NEXT ASSY	SCALE NONE SHEET 1 OF 1 SIZE C DWG. NO. CBL1451-101 REV. B

CBL1451-101 B

WIRE LIST			COMMENTS
FROM	TO	COLOR	
C1-07	T2	BLK	
C1-05	T1	RED	
C1-11	T4	WHT	
C1-21	T3	GRN	
C1-03	C1-01	RED	JMPR
C1-31	W1	RED	TP
C1-32	W2	BLK	
C1-37	W3	RED	
C1-39	W4	BLK	
C1-41	W5	WHT	
C1-43	W6	GRN	

LTR	DATE	REVISION	DR.	CK.
A	7/8/74	RELEASED	—	—
B	6/3/75	PER ECN 1606	JRB	JCH
C	9/15/75	PER ECN 1628	JRB	JCH



NOTES:-
1. STAMP MARKING C1 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY ITEM 6 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 4.
3. INSERT RETAINER ITEM 7 INTO SLOTS 9/10, 23/24 & 35/36.
4. INSTALL ITEM 10 IN CUTOUT OF ITEM 9 TO INSURE TIGHT FIT OF CABLE.
5. TYPE PART NO. & REVISION IN BLACK ON ITEM 14.
6. ALL UNUSED WIRES ARE TO BE CUT OFF AND TERMINATED INSIDE CABLE.
7. SEE DWG C INS1210 FOR CABLE CODING LOCATION.
8. FOR SIGNAL NAMES SEE LBD 1528
9. WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

-XXX	DIM L	TOL
-001	15 FT	± 6 IN.

I-06

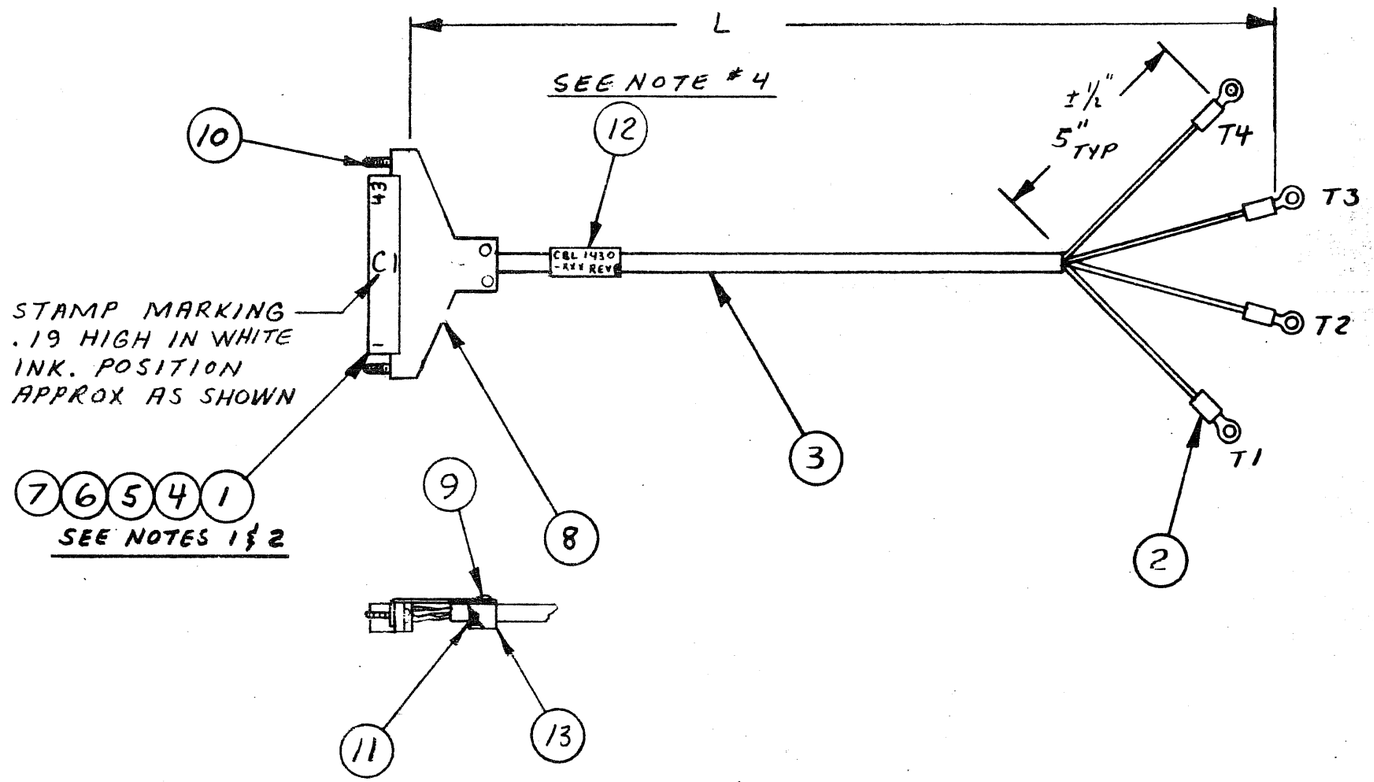
MATERIAL: SEE BOM	DWN: R. Bojan 5/14/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK: J. E. Thomas 7/12/74	CABLE, ASR TO SOC
	ENG: M. Spano 7-15-74	
	APPRD: [illegible]	
	USED ON	SCALE NONE SHEET 1 OF 1 SIZE C DWG. NO. CBL 1453-XXX REV. C
	NEXT ASSY	

DWG. NO. CBL1453-XXX REV. C

WIRE LIST

FROM	TO		COLOR	REMARKS
C1-7	T2		BLACK	
C1-5	T1		RED	
C1-11	T4		WHITE	
C1-21	T3		GREEN	
			BROWN	SEE NOTE 3
C1-3	C1-1		RED	JUMPER

LTR	DATE	REVISION	DR.	CK.
A	12/26/73	BOM PER ECN 1275	JCH	JCH
B	8/2/74	ITEM # 2, TITLE & P.N. PER ECN 1493	JCH	JSH
C	9/15/75	PER ECN 1628	NB	JCH



⚠ WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

NOTES:

1. INSERT RETAINER SPRING (ITEM #5) INTO SLOTS 9/10, 31/32 & 41/42
2. INSERT KEY (ITEM #7) BETWEEN SLOTS 25/26 & 27/28.
3. CUT-OFF UNUSED (BROWN) WIRE AT BOTH ENDS, TERMINATE INSIDE CABLE.
4. TYPE PART # & REV. IN BLK ON ITEM #12.

-002	15FT ± 6IN.
-001	25FT ± 1FT.
-XXX	"L" DIM.

MATERIAL: SEE BOM WAS CBL0C03

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES:
- DIMENSIONS ARE IN INCHES
- TOLERANCES

.XX	.XXX	ANGLES
± .02	± .005	± 1/2°

DWN J.C.H. 9/1/72
CHK JSH 8-6-74
ENG. Clark J. Crocker
APPRD
USED ON
NEXT ASSY 3101-001

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE, OPTION A OR SOC (TO 20 MA TELETYPE OR CRT) E.V.

SCALE NONE | SIZE B | DWG. NO. CBL1430-XXX | REV. C

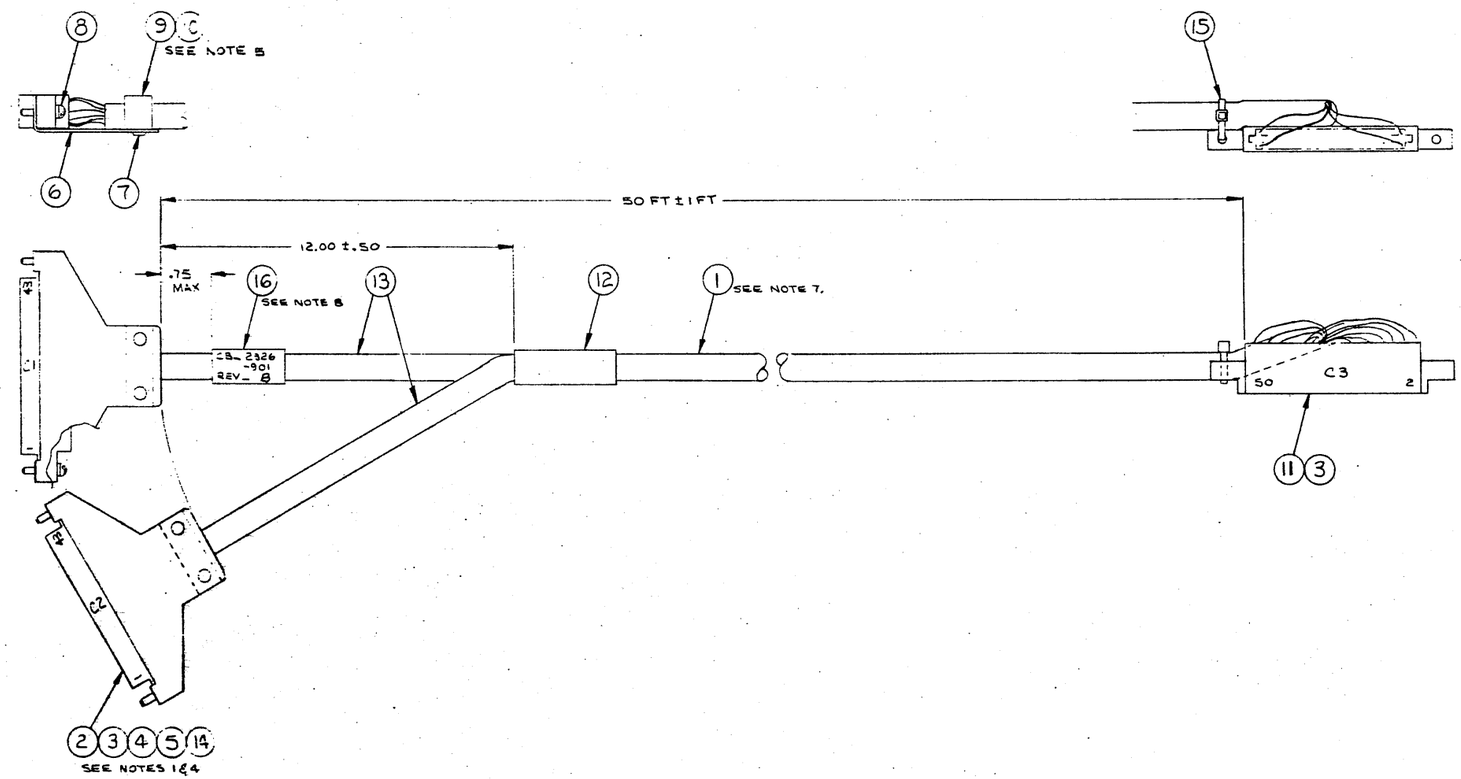
SHEET 1 OF 1

IV-06-B

M	LTR	DATE	REVISION	DR.	CK.
	A	9-8-75	RELEASED	PB.	JEE
	B	10/1/75	WIRE LIST PER ECN 1660	JCB	JEE

WIRE LIST

FROM	TO	WIRE COLOR	
C1-01	C3-22	BLACK	TP
02	21	WHITE	
03	34	YELLOW	
04	33	ORANGE	
05	38	GREEN	
06	37	GRAY	
07	30	BLK/WHT	
08	23	BLK/RED	
09	26	BLK/GRN	
10	25	BLK/ORG	
11	12	BLK/YEL	
12	11	BLK/BLU	
13	20	WHT/BLK	
14	19	WHT/RED	
15	16	WHT/GRN	
16	15	WHT/ORG	
35	50	GRN/WHT	
36	49	GRN/BLU	
33	28	GRN/BLK	
34	27	GRN/RED	
41	40	GRN/BRN	
C1-42	C3-39	GRN/YEL	TP
C2-09	C3-18	WHT/BLU	
10	17	WHT/YEL	
11	46	WHT/BRN	
12	45	WHT/GRA	
13	10	YEL/BLK	
14	09	YEL/RED	
15	42	YEL/GRN	
16	41	YEL/BLU	
13	01	YEL/BRN	
20	05	YEL/GRA	
23	04	ORG/BLK	TP
24	C3-05	ORG/RED	TP
35	C2-41	BLACK #28	SEE NOTE 3
43	C3-14	ORG/BRN	TP
44	3	ORG/GRA	
37	36	GRA/RED	
33	06	GRA/WHT	
21	02	GRA/YEL	TP
C2-39	C3-44	GRA/ORG	TP



NOTES

1. STAMP MARKINGS C1, C2 & C3 IN .19 HIGH NOTE CHARACTERS; LOCATE APPROX AS SHOWN.
2. .
3. USE ITEM 14 FOR BLACK #28 JUMPER.
4. INSERT KEY, ITEM 5, BETWEEN SLOTS 25/26 & 27/28 OF ITEM 2, 2 PLCS.
5. INSTALL ITEM 10 IN CUTOUT OF ITEM 9 TO PREVENT SLIPPAGE OF CABLE 2 PLCS.
7. CUT OFF ALL UNUSED WIRES FLUSH WITH OUTER JACKET, BOTH ENDS.
8. MARK PART NO. & REV IN BLACK ON ITEM 16.

V-07

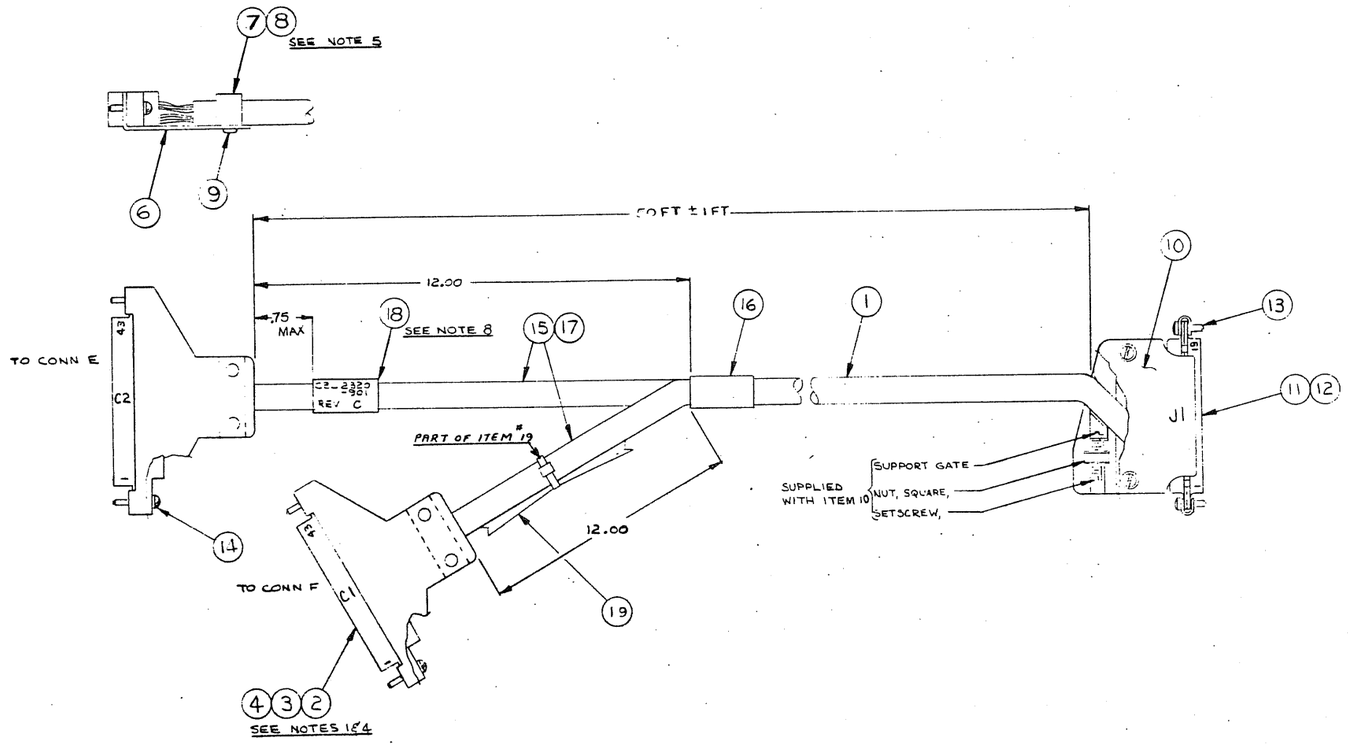
MATERIAL: SEE BOM	DWN: J.C. Bratman 7-25-75	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02, XXX ±.005, ANGLES ±1/2°	CHK: [illegible] 9/16/75	CABLE ASSY SOC-GOULD	
	ENG: [illegible] 9/16/75		
	APPRO.		
	USED ON: CBL2326-901	SCALE: NONE	SIZE: D DWG. NO. CBL2326-901 REV. B
	NEXT ASSY	SHEET OF 1	

CBL2326-901 B

M	LTR	DATE	REVISION	DR.	CK.
	A	9/12/75	RE-	DB	TBL
	B	9-11-75	ROW REDRAWN	RB	TBL
	C	12/2/75	REVISED PER ECR 1690	TBL	

WIRE LIST

FROM	TO	WIRE COLOR	
J1-01	J1-08	BLACK	TP
02	27	WHITE	
03	07	YELLOW	
04	26	ORANGE	
05	06	GREEN	
06	25	GRAY	
07	05	BLK/WHT	
08	24	BLK/RED	
09	04	BLK/GRN	
10	23	BLK/ORG	
11	03	BLK/YEL	
12	22	BLK/BLU	
13	02	WHT. BLK	
14	21	WHT/RED	
15	01	WHT/GRN	
16	20	WHT/ORG	TP
33	J1-32	GRN/BLK	* SEE NOTE 2
33	C2-19	GRN/BLK	
35	J1-10	GRN/WHT	TP
36	J1-29	GRN/BLU	
37	J1-11	GRN/BRN	* SEE NOTE 3
37	C1-41	BLACK #28	* WPR
41	C2-33	BLACK #28	WPR
38	J1-30	GRN/YEL	
39	12	GRN/GRA	TP
40	31	GRA/BLK	
43	18	GRA/YEL	TP
C1-44	J1-37	GRA/ORG	
C2-17	C2-18	BLACK #28	WPR
21	C2-33	BLACK #28	WPR
23	J1-19	YEL/GRN	
25	09	YEL/BRN	TP
26	28	YEL/GRA	
27	16	ORG/BLK	
28	35	ORG/RED	
29	15	ORG/GRN	
30	34	ORG/BLU	
31	17	ORG/BRN	
32	36	ORG/GRA	
39	14	GRA/RED	TP
C2-40	J1-33	GRA/WHT	
C2-39	C2-41	BLACK #28	WPR



NOTES

1. STAMP MARKINGS C1, C2 & J1 IN .19 HIGH WHITE CHARACTERS; LOCATE APPROX AS SHOWN.
2. * INDICATES DOUBLE CRIMP, USE ITEM 4, 3 PLCS
3. USE ITEM 17 FOR BLACK #28 JUMPERS. 4 PLCS.
4. INSERT KEY, ITEM 5, BETWEEN SLOTS 25/26 & 27/28 OF ITEM 2. 2 PLCS.
5. INSTALL ITEM 8 IN CUTOUT OF ITEM 7 TO PREVENT SLIPPAGE OF CABLE. 2 PLCS.
7. CUT OFF ALL UNUSED WIRES FLUSH WITH OUTER JACKET, BOTH ENDS.
8. MARK PART NO. & REV IN BLACK ON ITEM 18

MATERIAL: SEE BOM	DWN: [illegible] 7-24-75	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.01 .XXX ±.005 ANGLES ±1/2°	CHK: T.B. Blumenthal	CABLE ASSY SOC-VERSATEC
	ENG: [illegible] 8-27-75	
	APPRD: [illegible]	
USED ON: [illegible]	SCALE: NONE	SIZE: D DWG. NO. CBL2320-901 REV C
NEXT ASSY	SHEET OF	

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lador 10/20/75 | CHK. JCM 12/24/75 | ENG. M. Spodar 12-24-75 | APPRD. | STANDARD COST _____ DATE _____

TITLE: SOC ASSY E.V.
RTC/ALC/16 BIT BP
DMA/PIC
(BPIOC)

BOM 3007 **-XXX** REV. B
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JCM			
B	1729	KJ			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2057-901	1								PC BD SUB-ASSY, SOC, E.V.	
2	A	MEC 0292	1								LABEL, MODEL & SERIAL NO.	
3	A	MEC1721-108	2								RESISTOR, CAP DIP ASSY, RC108	
4	A	MEC1720-116	1								JUMPER, DIP ASSY W116	
5	A	MEC1720-117	1								W117	
6	A	MEC1720-139	1								W139	
7	A	MEC1720-140	1								W140	
8	A	MEC1720-142	1								W142	
9	A	MEC1720-145	1								W145	
10	A	MEC1720-146	1								W146	
11	A	MEC1720-150	1								W150	
12	A	MEC1720-155	1								W155	
13	A	MEC1720-161	1								JUMPER, DIP ASSY W161	
14		ICD0026	8								74H01	
15		RES0250-102	4								RESISTOR NETWORK, 1K, 16 PIN DIP	
	C	LBD2282	REF								LOGIC BLOCK DIAGRAM	A
	A	SPC 1831	REF.								SPEC., FUNCTIONAL	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lador 10/20/75 | CHK. JCM 12/24/75 | ENG. [illegible] 12-24-75 | APPRD. | STANDARD COST _____ DATE _____

TITLE: SOC ASSEMBLY
E.V.
RTC/AL/PTR-P
DMA/PIC

BOM 3006 **-XXX** REV. B
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JCM			
B	1729	KJ			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2057-901	1								PC BD SUB-ASSY, SOC, E.V.	
2	A	MEC0292	1								LABEL, MODEL & SERIAL NO.	
3	A	MEC1721-101	1								RESISTOR, CAP DIP ASSY RC101	
4	A	MEC1721-102	1								RESISTOR, CAP DIP ASSY RC102	
5												
6												
7	A	MEC1720-101	1								JUMPER, DIP ASSY W101	
8	A	MEC1720-102	1								W102	
9	A	MEC1720-141	1								W141	
10	A	MEC1720-143	1								W143	
11	A	MEC1720-147	1								W147	
12	A	MEC1720-151	1								W151	
13	A	MEC1720-152	1								W152	
14	A	MEC1720-157	1								W157	
15	A	MEC1720-160	1								W160	
16	A	MEC1720-163	1								JUMPER, DIP ASSY W163	
17		ICD0026	8								74H01	
18		RES0250-102	4								RESISTOR NETWORK, 1K, 16 PIN DIP	
	C	LBD2282	REF								LOGIC BLOCK DIAGRAM	A
	A	SPC 1831	REF								SPEC., FUNCTIONAL	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lador 10/20/75 | CHK. JCM 12/24/75 | ENG. [illegible] 12/24/75 | APPRD. | STANDARD COST _____ DATE _____

TITLE: SOC ASSY E.V.
GOULD

BOM 3008 **-XXX** REV. B
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JCM			
B	1729	KJ			
B1	1726				

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2057-901		1							PC BD SUB-ASSY, SOC, E.V.	
2	A	MEC 0292		1							LABEL, MODEL & SERIAL NO.	
3	A	MEC1721-117		1							RESISTOR, CAP DIP ASSY RC117	
4	A	MEC1721-118		1							RESISTOR, CAP DIP ASSY RC118	
5	A	MEC1720-134		1							JUMPER, DIP ASSY W134	
6	A	MEC1720-135		1							W135	
7	A	MEC1720-144		1							W144	
8	A	MEC1720-146		1							W146	
9	A	MEC1720-147		1							W147	
10	A	MEC1720-148		1							W148	
11	A	MEC1720-149		1							W149	
12	A	MEC1720-151		1							W151	
13	A	MEC1720-158		1							W158	
14	A	MEC1720-163		1							JUMPER, DIP ASSY W163	
15		ICD 0026		3							74H01	
16		RES0250-102		4							RESISTOR NETWORK, 1K, 16 PIN DIP	
17		ICD0029		3							74H08	
18		MEC1590-003		2							LABEL, I/O CONN IDENTIFICATION	B
	C	LBD2282		REF							LOGIC BLOCK DIAGRAM	A
	A			REF							SPEC., FUNCTIONAL	

PDF-004A SPC 2717

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lador 10/20/75 | CHK. JCM 12/24/75 | ENG. [illegible] 12/24/75 | APPRD. | STANDARD COST _____ DATE _____

TITLE: SOC ASSY E.V.
RTC/ALC/ DMA
PIC
VERSATEC

BOM 3009 **-XXX** REV. B1
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JCM			
B	1729	KJ			
B1	1726	JCM			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2057-901		1							PC BD SUB-ASSY, SOC E.V.	
2	A	MEC0292		1							LABEL, MODEL & SERIAL NO.	
3	A	MEC1721-116		1							RESISTOR, CAP DIP ASSY RC116	
4	A	MEC1720-135		1							JUMPER, DIP ASSY W135	
5	A	MEC1720-134		1							W134	
6	A	MEC1720-148		1							W148	
7	A	MEC1720-151		1							W151	
8	A	MEC1720-152		1							W152	
9	A	MEC1720-153		1							W153	
10	A	MEC1720-154		1							W154	
11	A	MEC1720-156		1							W156	
12	A	MEC1720-159		1							W159	
13	A	MEC1720-162		1							JUMPER, DIP ASSY W162	
14	A	MEC1288-021		1							RESISTOR, DIP ASSY R21	
15		ICD 0026		4							74H01	
16		RES0250-102		4							RESISTOR NETWORK, 1K, 16 PIN DIP	
17		ICD 0029		1							74H08	
18	A	MEC1720-133		1							JUMPER, DIP ASSY W133	
19	B	MEC1590-003		2							LABEL I/O CONN IDENTIFICATION	B1
	C	LBD2282		REF							LOGIC BLOCK DIAGRAM	A
				REF.							SPEC., FUNCTIONAL	

V-09

PDF-004A

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 7-29-75
CHK. [illegible] 8/1/75
ENG. [illegible] 8/8/75
APPRD. [illegible]
STANDARD COST _____ DATE _____

TITLE: SOC-GOULD ASSY
W.W.

BOM 3008 -XXX REV. D
NHA: SHT. 1 OF 4

REV.	ECN	CK	REV.	ECN	CK
A	REL	[illegible]	C,	1726	
A,	1651	[illegible]	D	1727	[illegible]
B	1643	[illegible]			
C	1725	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-	-	-	-	-	-	-	DESCRIPTION	STANDARD COST
1	D	MEC 2027-001	1								P.C. BOARD SOCKET ASSY	
2	C	MEC 0587	1								STIFFENER ASSY	
3		MEC 0356	5								WASHER, FIBRE	
4	A	MEC 0412 -	4								STANDOFF, PIN FIELD GUARD	
5	C	MEC 0270	1								PINFIELD GUARD	
6		MEC 0303-005	5								SCREW, BD HD *4-40 X 5/16 LG	
7		MEC 0309-004	10								SCREW, RD HD NYLON *4-40X5/16LG	
8		MEC 0388-002	5								NUT, SELF LOCKING	
9		RES 0250-153	2								RESISTOR NETWORK 15K	
10		RES 0250-471	2								RESISTOR NETWORK 470Ω	
11		RES 0250-102	3								RESISTOR NETWORK 1K	
12	A	MEC 1721-105	1								RESISTOR, CAP DIP ASSY RC105	
13	A	MEC 1721-106	1								RESISTOR, CAP DIP ASSY RC106	
14		ICD 0025	11								74H00	
15		ICD 0026	4								74H01	
16		ICD 0028	17								74H04	
17		ICD 0029	9								74H08	
18		ICD 0030	4								74H10	
19		ICD 0031	7								74H11	
20		ICD 0033	3								74H20	
21		ICD 0034	4								74H21	
22		ICD 0035	2								74H30	

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B.
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: SOC-GOULD ASSY
WW

BOM 3008 -XXX REV. D
NHA: SHT. 2 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-	-	-	-	-	-	-	DESCRIPTION	STANDARD COST
23		ICD 0038	4								74H50	
24		ICD 0039	3								74H52	
25		ICD 0040	4								74H53	
26		ICD 0043	4								74H74	
27		ICD 0046	1								74H106	
28		ICD 0047	1								74150	
29		ICD 0048	2								74151	A
30		ICD 0049	9								74153	
31		ICD 0050	5								74155	
32		ICD 0051	16								74157	
33		ICD 0052	6								74161	
34		ICD 0053	14								74174	
35		ICD 0054	17								74175	
36		ICD 0058	4								7442	
37		ICD 0059	1								8094	
38		ICD 0060	6								8262	
39		ICD 0062	7								9602	
40		ICD 0067	2								1488	
41		ICD 0068	3								1489	
42		ICD 0069	2								7432	
43		ICD 0072	11								745112	
44		ICD 0083	1								74158	

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B.
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: SOC-GOULD ASSY
WW

BOM 3008 -XXX REV. D
NHA: SHT. 3 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-	-	-	-	-	-	-	DESCRIPTION	STANDARD COST
45		ICD 0112	7								8095	
46		ICD 0113	1								7438	
47		ICD 0186	1								74154	
48		ICD 0191	14								7408	
49		ICD 0194	11								7400	
50		ICD 0195	6								7404	
51		ICD 0196	3								7410	
52		ICD 0198	1								7420	
53		ICD 0201	25								7474	A
54		ICD 0215	2								74H55	
55		ICD 0582	4								8225	
56		ICD 0664	2								7414	
57		ICD 1253	1								PSAR (PR1472B)	
58		ICD 1254	1								PSAT (PT1482B)	
59		ICD 1681	4								7497	
60		ICD 0027	1								7402	
61		ICD 1760	2								745253	
62		ICD 0185	1								74148	
63		ICD 0044	1								7486	
64	A	MEC 1721-107	1								RESISTOR CAP ASSY RC107	
65		ICD 0079	2								82562	
66	A	MEC 1721-117	1								RESISTOR CAP ASSY RC117	

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B.
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: SOC-GOULD ASSY
WW

BOM 3008 -XXX REV. D
NHA: SHT. 4 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
67	A	MEC 1720-131	1								JUMPER DIP ASSY W131	
68	A	MEC 1720-134	1								JUMPER DIP ASSY W134	
69	A	MEC 1720-135	1								JUMPER DIP ASSY W135	
70	A	MEC 1720-136	1								JUMPER DIP ASSY W136	
71	A	MEC 1720-137	1								JUMPER DIP ASSY W137	
72	A	MEC 1720-138	1								JUMPER DIP ASSY W138	
73	A	MEC 1264-010	2								JUMPER DIP ASSY W-10	
74	A	MEC 1721-118	1								RESISTOR CAP ASSY RC118	
75	A	MEC 0292	1								LABEL, MODEL & SERIAL NO.	
76	B	MEC 2370-001	1								LABEL, ECN LOG	A
77	B	MEC 1590-003	2								LABEL, I/O CONN. IDENTIFICATION	A

PRIME COMPUTER INC. NATICK MASS.

DWN. [illegible] 5/30/75 | CHK. [illegible] | ENG. [illegible] 5/27/75 | APPRD

STANDARD COST _____ DATE _____

TITLE: VERSATEC SOC ASSEMBLY RTC/ALC/DMA/PIC — WW

BOM 3009-XXX REV. D — NHA: — SHT. 1 OF 4

REV.	ECN	CK	REV.	ECN	CK
A	[illegible]	[illegible]	C	1725	[illegible]
A1	1651	[illegible]	C1	1726	
B	1693	[illegible]	D	1727	[illegible]
B1	1704	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
1	D	MEC 2027-001	1	P.C. BOARD SOCKET ASSY	
2	C	MEC 0587	1	STIFFENER ASSY	
3		MEC 0356	5	WASHER, FIBRE	
4	A	MEC 0412	4	STANDOFF, PIN FIELD GUARD	
5	C	MEC 0270	1	PINFIELD GUARD	
6		MEC 0303-005	5	SCREW, BD HD #4-40 X 5/16 LG	
7		MEC 0303-004	10	SCREW, RD HD NYLON #4-40 X 3/16 LG	
8		MEC 0382-002	5	NUT, SELF LOCKING	
9		RES 0250-153	2	RESISTOR NETWORK 15K	
10		RES 0250-471	2	RESISTOR NETWORK 470 Ω	
11		RES 0250-102	3	RESISTOR NETWORK 1K	
12	A	MEC 1721-105	1	RESISTOR, CAP DIP ASSY RC105	
13	A	MEC 1721-106	1	RESISTOR, CAP DIP ASSY RC106	
14		ICD 0025	11	74H00	
15		ICD 0026	5	74H01	
16		ICD 0028	17	74H04	
17		ICD 0029	7	74H08	
18		ICD 0030	4	74H10	
19		ICD 0031	7	74H11	
20		ICD 0033	3	74H20	
21		ICD 0034	4	74H21	
22		ICD 0035	2	74H30	

PRIME COMPUTER INC. NATICK MASS.

DWN. [illegible] 5/30/75 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: VERSATEC SOC ASSEMBLY — WW

BOM 3009-XXX REV. D — NHA: — SHT. 2 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
23		ICD 0038	4	74H50	
24		ICD 0039	3	74H52	
25		ICD 0040	4	74H53	
26		ICD 0043	4	74H74	
27		ICD 0046	1	74H106	
28		ICD 0047	1	74150	
29		ICD 0048	2	74151	⚠
30		ICD 0049	9	74153	
31		ICD 0050	5	74155	
32		ICD 0051	16	74157	
33		ICD 0052	6	74161	
34		ICD 0053	14	74174	
35		ICD 0054	17	74175	
36		ICD 0058	4	7442	
37		ICD 0059	1	8094	
38		ICD 0060	6	8262	
39		ICD 0062	7	9602	
40		ICD 0067	2	1488	
41		ICD 0068	3	1489	
42		ICD 0069	2	7492	
43		ICD 0072	11	743112	
44		ICD 0083	1	74158	

PRIME COMPUTER INC. NATICK MASS.

DWN. [illegible] 5/30/75 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: VERSATEC SOC ASSEMBLY — WW

BOM 3009-XXX REV. D — NHA: — SHT. 3 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
45		ICD 0112	7	8095	
46		ICD 0113	1	7438	
47		ICD 0186	1	74154	
48		ICD 0191	14	7408	
49		ICD 0194	11	7400	
50		ICD 0195	6	7404	
51		ICD 0196	3	7410	
52		ICD 0198	1	7420	
53		ICD 0201	25	7474	⚠
54		ICD 0215	2	74H55	
55		ICD 0582	4	8225	
56		ICD 0664	2	7414	
57		ICD 1253	1	PSAR (PR1472B)	
58		ICD 1254	1	PSAT (PT1482B)	
59		ICD 1681	4	7497	
60		ICD 0027	1	7402	
61		ICD 1760	2	745253	
62		ICD 0185	1	74148	
63		ICD 0044	1	7486	
64		MEC 1721-107	1	RESISTOR CAP ASSY RC107	
65		ICD 0079	2	82562	
66	A	MEC 1264-014	1	JUMPER DIP ASSY W14	

PRIME COMPUTER INC. NATICK MASS.

DWN. [illegible] 5/30/75 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: VERSATEC SOC ASSEMBLY — WW

BOM 3009-XXX REV. D — NHA: — SHT. 4 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
67	A	MEC 1264-010	1	JUMPER DIP ASSY W10	
68	A	MEC 1288-021	1	RESISTOR DIP ASSY R21	
69	A	MEC 1720-131	2	JUMPER DIP ASSY W131	
70	A	MEC 1720-132	1	JUMPER DIP ASSY W132	
71	A	MEC 1720-133	1	JUMPER DIP ASSY W133	
72	A	MEC 1720-134	1	JUMPER DIP ASSY W134	
73	A	MEC 1720-135	1	JUMPER DIP ASSY W135	
74	A	MEC 1720-107	1	JUMPER DIP ASSY W107	
75	A	MEC 1721-116	1	RESISTOR CAP ASSY RC116	
76	A	MEC 0292	1	LABEL, MODEL & S.N.	⚠
77	B	MEC 2370-001	1	LABEL, ECN LOG	⚠
78	B	MEC 1590-003	2	LABEL, I/O CONN. IDENTIFICATION	⚠
	D	LBD 1528	REF	LOGIC BLOCK DIAGRAM	

PRIME COMPUTER INC. NATICK MASS.

DWN. W.A.B 5/3/74 | CHK. J.C.L. 7/14/74 | ENG. M.S. 7-15-74 | APPRD. [signature]

STANDARD COST _____ DATE _____

TITLE: SOC SUB ASSEMBLY WW

BOM MEC 2036 -XXX REV. G

NHA: 3006 / 3007 SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL	—	E	1586	MS
B	1459/1461	MS	F	1626	MS
C	1523/1524	JCL	F1	1651	JCL
D	1548	MS	G	1727	KL

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	MEC 2027-001	1								P.C. BOARD SOCKET ASSY	
2	C	MEC0587	1								STIFFENER ASSY	
3		MEC 0356	5								WASHER, FIBRE	
4	A	MEC 0412	4								STANDOFF, PIN FIELD GUARD	
5	C	MEC 0270	1								PINFIELD GUARD	
6		MEC 0303-005	5								SCREW, BD HD #4-40 X 5/16 LG	
7		MEC 0309-001	10								SCREW, RD HD NYLON #4-40 X 5/16 LG	
8		MEC 0329 001	5								NUT, SELF LOCKING	
9		RES 0250-153	2								RESISTOR NETWORK 15K	
10		RES 0250-471	2								RESISTOR NETWORK 470Ω	
11		RES 0250-102	3								RESISTOR NETWORK 1K	
12	A	MEC 1721-105	1								RESISTOR, CAP DIP ASSY RC105	
13	A	MEC 1721-106	1								RESISTOR, CAP DIP ASSY RC106	
14		ICD 0025	11								74H00	
15		ICD 0026	9								74H01	
16		ICD 0028	17								74H04	
17		ICD 0029	6								74H08	
18		ICD 0030	4								74H10	
19		ICD 0031	7								74H11	
20		ICD 0033	3								74H20	
21		ICD 0034	4								74H21	
22		ICD 0035	2								74H30	A

P07-004A

PRIME COMPUTER INC. NATICK MASS.

DWN. J.K.E 5/3/74 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: SOC SUB ASSEMBLY WW

BOM MEC 2036 -XXX REV. G

NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
23		ICD 0038	4								74H50	
24		ICD 0039	3								74H52	
25		ICD 0040	4								74H53	
26		ICD 0043	4								74H74	
27		ICD 0046	1								74H106	
28		ICD 0047	1								74150	
29		ICD 0048	1								74151 A	
30		ICD 0049	9								74153	
31		ICD 0050	5								74155	
32		ICD 0051	16								74157	
33		ICD 0052	6								74161 B E	
34		ICD 0053	14								74174 B D	
35		ICD 0054	17								74175	
36		ICD 0058	4								7442	
37		ICD 0059	1								8094	
38		ICD 0060	6								8262 A	
39		ICD 0062	7								9602	
40		ICD 0067	2								1488	
41		ICD 0068	3								1489	
42		ICD 0069	2								7432	
43		ICD 0072	11								745112	
44		ICD 0083	1								74158	

P07-004A

PRIME COMPUTER INC. NATICK MASS.

DWN. J.K.E 5/3/74 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: SOC SUB ASSEMBLY WW

BOM MEC 2036 -XXX REV. G

NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

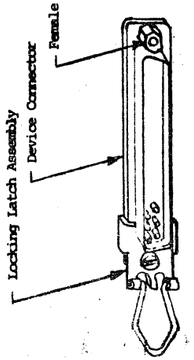
ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
45		ICD 0112	7								8095	
46		ICD 0113	1								7438	
47		ICD 0186	1								74154	
48		ICD 0191	14								7408	
49		ICD 0194	11								7400	
50		ICD 0195	6								7404	
51		ICD 0196	3								7410	
52		ICD 0198	1								7420	
53		ICD 0201	24								7474	
54		ICD 0215	2								74H55	
55		ICD 0582	4								8225	
56		ICD 0664	2								7414	
57		ICD 1253	1								PSAR (PR1472B)	
58		ICD 1254	1								PSAT (PT1482B)	
59		ICD 1681	4								7497	
60		ICD 0027	1								7402	
61		ICD 1760	2								745253	
62		ICD0185	1								74148 B	
63		ICD 0044	1								7486	
64		MEC 1721-107	1								RESISTOR CAP ASSY RC107	
65		ICD0079	2								82562 A	
66	B	MEC 2370-001	1								LABEL, ECN LOG	A

P07-004A

LTR	DATE	REVISION	DR.	CK.
A	12/8/75	RELEASED	JCL	TCL

Installation Procedure

The Versatec device cable connector locking mechanism must be changed to accomodate the screwlock assembly supplied with this cable, in this kit. To accomplish this, the locking latch assembly (see detail A) must be removed and replaced by the screwlock assemblies supplied.



DETAIL A

PRIME COMPUTER INC.
NATICK, MASS.

VERSATEC CABLE
INSTALLATION DRAWING

DWN.	CHK.	ENG.	APPRD.	SIZE	DWG. NO.	REV.
12/2/75	12/3/75	12/9/75	12/12/75	A	INS 2433	A

MATERIAL

UNLESS OTHERWISE SPECIFIED
-REMOVE ALL BURRS AND SHARP EDGES
-DIMENSIONS ARE IN INCHES
-TOLERANCES
XX ±.02 XXX ±.005 ANGLES ±1/2°

USED ON CBL 2390-XXX | SCALE NONE | SHEET 1 OF 1
NEXT ASSY KIT 2432-901

PRIME COMPUTER INC.
NATICK MASS.

DWN. P. Bigelow 7-25-75
CHK. TCL 8/9/75
ENG. K. Lupo 8/11/75
APPRD. [illegible]

TITLE: CABLE ASSY SOC-GOULD

BOM CBL 2326 -XXX REV. B
NHA: 3008-901 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	[illegible]			
B	1660	[illegible]			

STANDARD COST _____ DATE _____

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1		WIR1420	50'								CABLE, 22 T.P. #28 COLOR CODED	
2	B	CON0019	2								CONNECTOR HOUSING, 44 PIN	
3		CON0163	82								CONTACT, CRIMP 28-24 AWG	
4												
5		CON0210	2								KEY, POLARIZING	
6	B	MEC1236-001	2								BRACKET, CABLE CLAMP	
7		MEC0407	4								EYELET, FLAT FLANGE	
8	A	MEC0311-001	4								SCREW, CAPTIVE	
9	B	MEC1237-001	2								BLOCK, CABLE CLAMP	
10		MEC0420-001	A/R								TAPE, DOUBLE COATED, 3/8W	
11		CON0205-025	1								CONNECTOR HOUSING, 50 PIN	
12		MEC0159-009	.5'								TUBING, HT. SHR. 3/4 ID	
13		MEC0540-006	2'								SLVG, INSUL 5/16 ID	
14		WIR0241-001	2"								WIRE, STRANDED, #28 BLK	
15		MEC0182-002	1								CABLE TIE	
16	A	MEC0421	1								MARKER, CABLE	

PSF-004A

PRIME COMPUTER INC.
NATICK MASS.

DWN. P. Bigelow 9-11-75
CHK. TCL 9/11/75
ENG. K. Lupo 9-11-75
APPRD. [illegible]

TITLE: CABLE ASSY SOC-VERSATEC

BOM CBL 2320 -XXX REV. C
NHA: 3009 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	TCL			
B	REDWN	TCL			
C	1690	[illegible]			

STANDARD COST _____ DATE _____

ITEM	SIZE	PART NUMBER	QUANTITY -901	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1		WIR1420	50'								CABLE, 22 T.P. #28 COLOR CODED	
2	B	CON0019	2								CONNECTOR HOUSING 44 PIN	
3		CON0163	44								CONTACT, CRIMP 28-24 ANG	
4		CON0251	3								CONTACT CRIMP, 24-20 AWG	
5		CON0210	2								KEY, POLARIZING	
6	B	MEC1236-001	2								BRACKET, CABLE CLAMP	
7	B	MEC1237-001	2								BLOCK, CABLE CLAMP	
8		MEC0420-001	A/R								TAPE, DOUBLE COATED 3/8W	
9		MEC0407-001	4								EYELET, FLAT FLANGE	
10		CON0228-037	1								CONNECTOR HOUSING	
11		CON0543-037	1								CONNECTOR, 37 PIN JI	
12		CON0544-002	36								CONTACT, CRIMP, SOCKET, 24-28 AWG	
13		MEC0312	1								MALE SCREW RETAINER KIT	
14		MEC0311-001	4								SCREW, CAPTIVE	
15		MEC0540-006	1.5'								SLVG, INSUL. PVC 5/16 I.D.	
16		MEC0159-005	.5'								SLVG, INSUL. H.S. 3/8 I.D.	
17		WIR0241-001	3'								WIRE, STRANDED, #28 BLK	
18	A	MEC0421	1								MARKER, CABLE	
19		KIT2432-901	1								KIT, VERSATEC CABLE INSTALLATION	

PSF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [illegible] 12/2/75
CHK. TCL 12/9/75
ENG. K. Lupo 12/11/75
APPRD. [illegible] 12/11/75

TITLE: KIT, VERSATEC CABLE INSTALLATION

BOM KIT 2432 -XXX REV. A
NHA: CBL 2320-901 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	TCL			

STANDARD COST _____ DATE _____

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1		MEC 0389	1								NUT, SCREWLOCK KIT (FEMALE)	
2		MEC 0182-002	1								CABLE TIE	
3	A	INS 2433	1								VERSATEC CABLE INSTALLATION DWG	
4		REF	1								PLASTIC FILM BAG	